Design Guide

VT82C694X Apollo Pro133A with VT82C686A South Bridge

Preliminary Revision 0.5
November 19, 1999
VIA TECHNOLOGIES, INC.

Copyright Notice:

VT82C585, VT82C586B, VT82C587, VT82C590, VT82C595, VT82C596B, VT82C597, VT82C598, VT82C680, VT82C685, VT82C686B, VT82687, VT82C691, VT82C693, VT82C693A, VT82C694, VT82C694X, VT8501, VT8601, Super South, Apollo VP, Apollo VPX, Apollo VP2, Apollo VP3, Apollo MVP3, Apollo MVP4, Apollo P6, Apollo Pro, Apollo Pro133, Apollo Pro 133A, and Apollo ProMedia may only be used to identify products of VIA Technologies.

Disclaimer Notice:

No license is granted, implied or otherwise, under any patent or patent rights of VIA Technologies. VIA Technologies makes no warranties, implied or otherwise, in regard to this document and to the products described in this document. The information provided by this document is believed to be accurate and reliable to the publication date of this document. However, VIA Technologies assumes no responsibility for any errors in this document. Furthermore, VIA Technologies assumes no responsibility for the use or misuse of the information in this document and for any patent infringements that may arise from the use of this document. The information and product specifications within this document are subject to change at any time, without notice and without obligation to notify any person of such change.

Offices:

USA Office:
1045 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301

Taipei Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453

Online Services:

Home Page: http://www.via.com.tw (Taiwan) –or- http://www.viatech.com (USA)
FTP Server: ftp.via.com.tw (Taiwan)
BBS: 886-2-22185208

REVISION HISTORY

Document Release	Date	Revision	Initials
0.5	11/19/99	Initial Release (Modified from DG694X&596BR070 and DG693A&686AR060)	VL, JY, VH, RC, SS

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

This document provides design guidelines for motherboard manufacturers on developing single Slot-1 or Socket-370 processor and Apollo Pro133A (VT82C694X) based systems. All the major underlying subsystems, especially Host Interface and Memory subsystems, related to the motherboard design are described in detail. General layouts, routing guidelines and power requirements of each subsystem are presented.

1.1 About This Design Guide

A brief description of each chapter is given below:

Chapter 1: Introduction.

An overview of Apollo Pro133A reference design features is given in this chapter along with general recommendations on Pro133A system design.

Chapter 2: Motherboard Design Guidelines.

General design schemes and recommended layout rules are shown in chapter 2. It begins with the 510-pin BGA ballout assignment. The following sections contain placement and routing of a motherboard, PCB stack-up information and power requirements for a desktop or a mobile system. Detailed placement, layout, and routing guidelines for each bus or subsystem (Host bus, Memory subsystem, AGP bus and PCI bus) are described in section 2.4.

Chapter 3: Timing Diagram Analysis.

133 MHz timing analyses for memory read/write cycles are discussed in Chapter 3.

Chapter 4: Electrical Specifications.

The electrical specifications for the VT82C694X North Bridge are listed in this chapter.

Chapter 5: Signal Connectivity and Design Checklist.

The final chapter provides signal connection tables as a brief reference for hardware design engineers who are experienced in PC motherboard design. Also design checklists are included that can be used for reviewing Pro133A system designs.

Appendices: Reference Design Schematics.

Appendix A shows two power-up strapping circuits for the VT82C686A SPKR pin which determines the function of the Secondary IDE disk data bus pins (SDD[15..0]) to be either SDD[15..0] (SPKR strapped low) or Audio/Game port functions (SPKR strapped high).
Appendix B describes the Printed Circuit Board (PCB) layout recommendations for VIA VT1611A (AC'97 audio codec) and Game/MIDI port in a motherboard design.
Reference schematics for an Apollo Pro133A system design with VT82C686A South Bridge are shown in Appendix C.

1.2 Apollo Pro133A Chipset Overview

The Apollo Pro133A chip set consists of the VT82C694X system controller (510-pin BGA) and the VT82C686A PCI to ISA bridge (352-pin BGA). The features for both chips are listed below and a typical system block diagram is shown in this section.

1.2.1 VT82C694X Apollo Pro133A North Bridge Features

Apollo Pro133A (VT82C694X) is a Slot-1 and Socket-370 system logic north bridge with the addition of 133 MHz capability for both the CPU and SDRAM interfaces. Apollo Pro133A may be used to implement both desktop and notebook personal computer systems from 66MHz to 133MHz based on 64-bit Slot-1 (Intel Pentium-II) and Socket-370 (Intel and Celeron) processors. The primary features of the Apollo Pro133A-North Bridge are:

- Slot-1 or Socket-370 CPU (Front Side Bus) Interface (66 / 100 / 133MHz)
- DRAM Memory Interface (66 / 100 / 133MHz)
- AGP Bus Interface (66MHz)
- PCI Bus Interface (33MHz)
- Mobile Power Management
- 510-pin BGA Package

The DRAM interface supports eight banks of DRAMs (4 DIMM sockets) although VIA recommends implementation of three DIMMs maximum for operation of the memory interface at 133 MHz. Total memory supported is 1.5 GB independent of the number of DIMMs implemented. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM controller can run synchronous with the host CPU bus (66 /100 /133 MHz) or synchronous / pseudo-synchronous with the AGP bus (66 / 133 MHz) with built-in PLL timing control. The DRAM interface can also run either slower or faster than the CPU interface (both combinations of 66 / 100 MHz or both combinations of 100 / 133 MHz).

The AGP controller supports full AGP v2.0 capability for maximum bus utilization including 2x and 4X mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT82C694X supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

For sophisticated power management, the Apollo Pro133A provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT82C686A south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

1.2.2 Super South (VT82C686A) Chipset Features

The VT82C686A Super-IO PCI Integrated Peripheral Controller (PSIPC) is a high integration, high performance, power efficient and high compatibility device that supports Intel and non-Intel based processors plus PCI bus bridge functionality to make a complete Microsoft PC98-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C686A includes the following standard intelligent peripheral controllers:

- Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands
- 4-Port Universal Serial Bus (USB) controller that is USB v1.1 and Universal HCI v1.1 compliant
- Keyboard controller with PS2 mouse support
- Real Time Clock (RTC) with 256 bytes extended CMOS
- Power management (PM) functionality compliant with ACPI and legacy APM requirements
- Hardware monitoring subsystem for managing system/motherboard voltage levels, temperatures, and fan speed
- Full System Management Bus (SMBus) interface
- Two 16550-compatible serial I/O ports with infrared communication port option
- Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system.
- Two game ports and one MIDI port
- ECP/EPP-capable parallel port
- Standard Floppy Disk Drive (FDD) interface
- Distributed DMA capability for support of ISA legacy DMA over the PCI bus. Serial IRQ is also supported for docking and non-docking applications
- Plug and play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel

1.2.3 System Block Diagram

A block diagram of a typical Apollo Pro133A based system with a VT82C686A South Bridge is shown in Figure 1-1. The Apollo Pro133A supports a single processor including 64-bit Slot-1 (Intel Pentium II ™) or Socket-370 (Intel Celeron ™) CPUs at 66 MHz, 100 MHz or the maximum 133MHz system bus frequency.

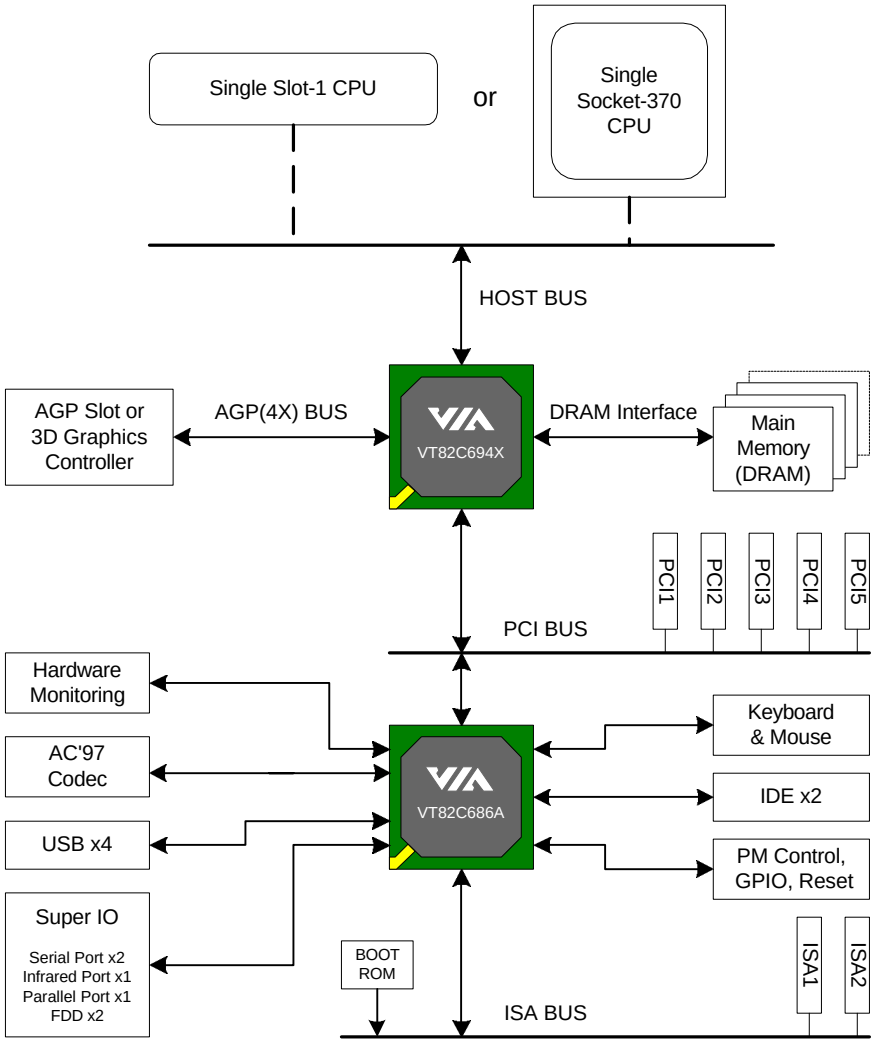


Figure 1-1. Apollo Pro133A System Block Diagram Using the VT82C686A South Bridge

1.3 System Design Recommendations

The VT82C694X Apollo Pro133A north bridge and VT82C686A south bridge form one of VIA's most optimized chipset combinations for single Slot-1or Socket-370 based PC systems. On an ATX form factor, for example, the optimized system specification for such a combination is listed below:

- Single Slot-1 or Socket-370 CPU (66 / 100 / 133MHz)
- Apollo Pro133A single chip clock synthesizer
- Apollo Pro133A North Bridge (Host/PCI) Controller
- VT82C686A South Bridge (PCI/ISA) Controller
- Four DIMM Slots (maximum 2 GB and 133MHz memory frequency)
- One AGP Slot (66MHz)
- Two PCI Slots (33MHz)
- One ISA Slots (8/16MHz)
- One AMR Slot (24.576MHz)
- One 2MB Flash ROM for system BIOS
- One AC'97 Codec Chip (VT1611) to cooperate with an AC'97 Link Controller
- Four Universal Serial Bus Ports
- PS2 Keyboard/Mouse Support
- Two Enhanced IDE Interfaces supporting both ATA-33 and ATA-66
- One Floppy Drive Interface
- One Infrared Interface
- Various Hardware Monitoring functions supporting 5 positive voltages, 3 temperatures, and 2 fan-speed inputs
- One Parallel Port and Two Serial Ports
- Three Audio Jacks including Audio In, Audio Out and Mic In
- One MIDI Port
- One Game Port

For the rest of this document, the specification above will be used as a reference example for component placement and PCB layout.

MOTHERBOARD DESIGN GUIDELINES

This chapter describes general design schemes and recommended layout rules. It begins with the 510-pin BGA (Pro133A north bridge) and 352-pin BGA (south bridge) ballout assignments. The following section contains the placement and routing of a motherboard, PCB stack-up information and power requirements for a desktop system. Detailed placement, layout, and routing guidelines for each bus or subsystem (Host bus, Memory subsystem, AGP bus and PCI bus) are described in section 2.4.

2.1 Ballout Assignment

Basically, the chipset ballout plays an important role in motherboard designs. It can determine the quality of the Printed Circuit Board (PCB) layout. The reliability of a motherboard partially depends on the ballout of both the North Bridge and the South Bridge. To achieve a cost effective and compact 4-layer motherboard, the ballouts should be well defined because they have an inseparable relationship with component placement and PCB layout.

2.1.1 Apollo Pro133A North Bridge Ballout Assignment

Ballout of the Apollo Pro133A North Bridge is designed to minimize the number of crossover signals. Figure 2-1 shows the four major signal group quadrants of the Apollo Pro133A Ballout. They are Host, Memory, AGP and PCI interfaces. Please refer to the VT82C694X datasheet for more details on ball assignments.

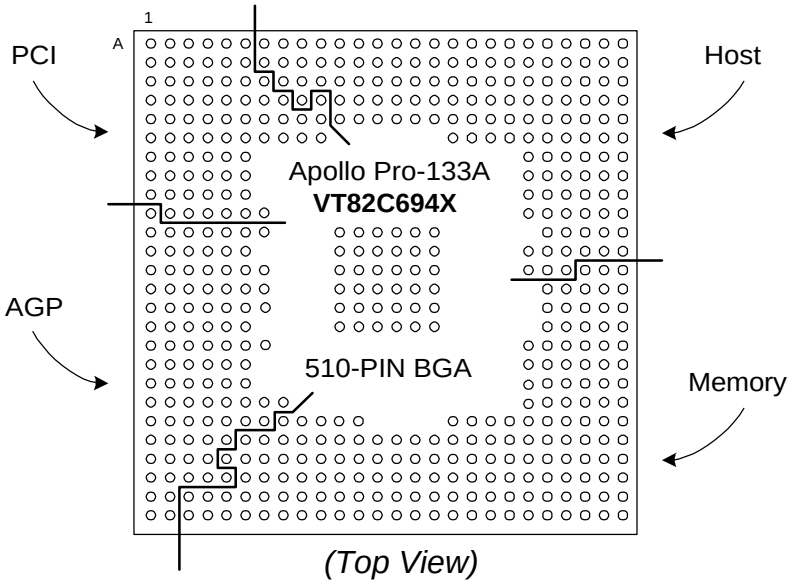


Figure 2-1. Major Signal Group Distributions of the Apollo Pro133A Ballout (Top View)

2.1.2 "Super South" South Bridge Ballout Assignment

Ballout of the VIA "Super South" South Bridge is designed to minimize the number of crossover signals. Similarly to Figure 2-1, the major signal group quadrants are shown in Figure 2-2. They are PCI, ISA, Hardware Monitoring, IDE1, IDE2 (shared with Audio/Game), Super IO (including FDC, COM, LPT, and Infrared interface (not shown)), USB, Keyboard & Mouse, and a group of Power Control, GPIO & Reset. Please refer to the VT82C686A datasheet for more details on these ball assignments.

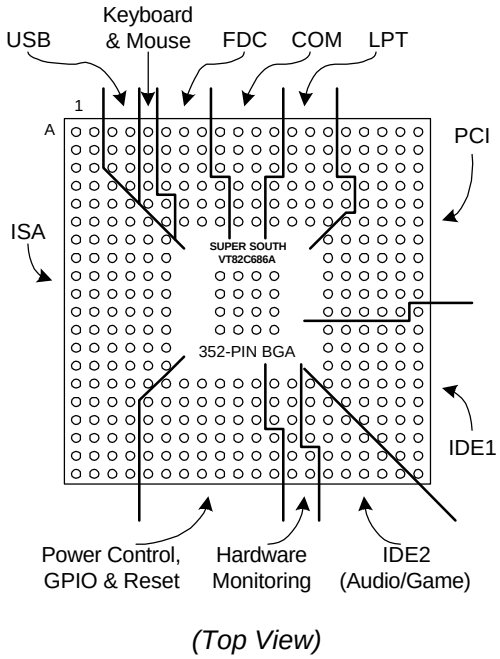


Figure 2-2. Major Signal Group Distributions of "Super South" South Bridge Ballout (Top View)

Package Information:

- The VIA VT82C694X Apollo Pro133A North Bridge is a 510-pin Ball Grid Array (BGA) package. The package size is 35mm x 35mm and the grid matrix is 26x26.
- The VIA "Super South" South Bridge (VT82C686A) is a 352-pin BGA package. The package size is 27mm x 27mm and the grid matrix is 20x20.

2.2 Motherboard Description

This section illustrates proposed component placements for an Apollo Pro133A based motherboard with different system configurations to achieve maximum optimization. The description of the Printed Circuit Board (PCB) for a motherboard is also given.

2.2.1 Slot-1 Motherboard Placement and Routing

For Slot-1 CPU and Apollo Pro133A PC motherboard designs, two proposed placements and group signal routings for the two most popular form factors (ATX and micro-ATX) are shown in figures 2-3 and 2-4 respectively. Detailed layout guidelines and signal routings for the Pro133 chipset will be addressed later in section 2.4.

Each figure shows a full size of its respective form factor. The empty area at the bottom of each placement diagram can be eliminated to reduce the board size. Table 2-1 shows the full size and the suggested compact size for each form factor implementation.

Table 2-1. Different Board Size Lists for Slot-1 System

Form Factor Type	Full size	Compact Size	Specification
ATX	12" x 9.6" (30.5cm x 24.5cm)	12" x 7.9" (30.5cm x 20cm)	1 AGP, 5 PCI, 1 ISA, 1 AMR, 3 DIMM
Micro-ATX	9.6" x 9.6" (24.5cm x 24.5cm)	9.6" x 7.9" (24.5cm x 20cm)	1 AGP, 2 PCI, 1 ISA, 1 AMR, 2 DIMM

2.2.1.1 ATX Form Factor for Slot-1 System

A proposed component placement and signal group routing for an Apollo Pro133A ATX form factor system design is illustrated in Figure 2-3. The major components on the board are single Slot-1 CPU, five PCI slots, one AMR, one ISA slot and three DIMM slots. This figure shows an ATX motherboard placement as a reference only. The placement should be re-evaluated if a different combination of AGP, PCI and ISA slots and other motherboard peripherals is desired.

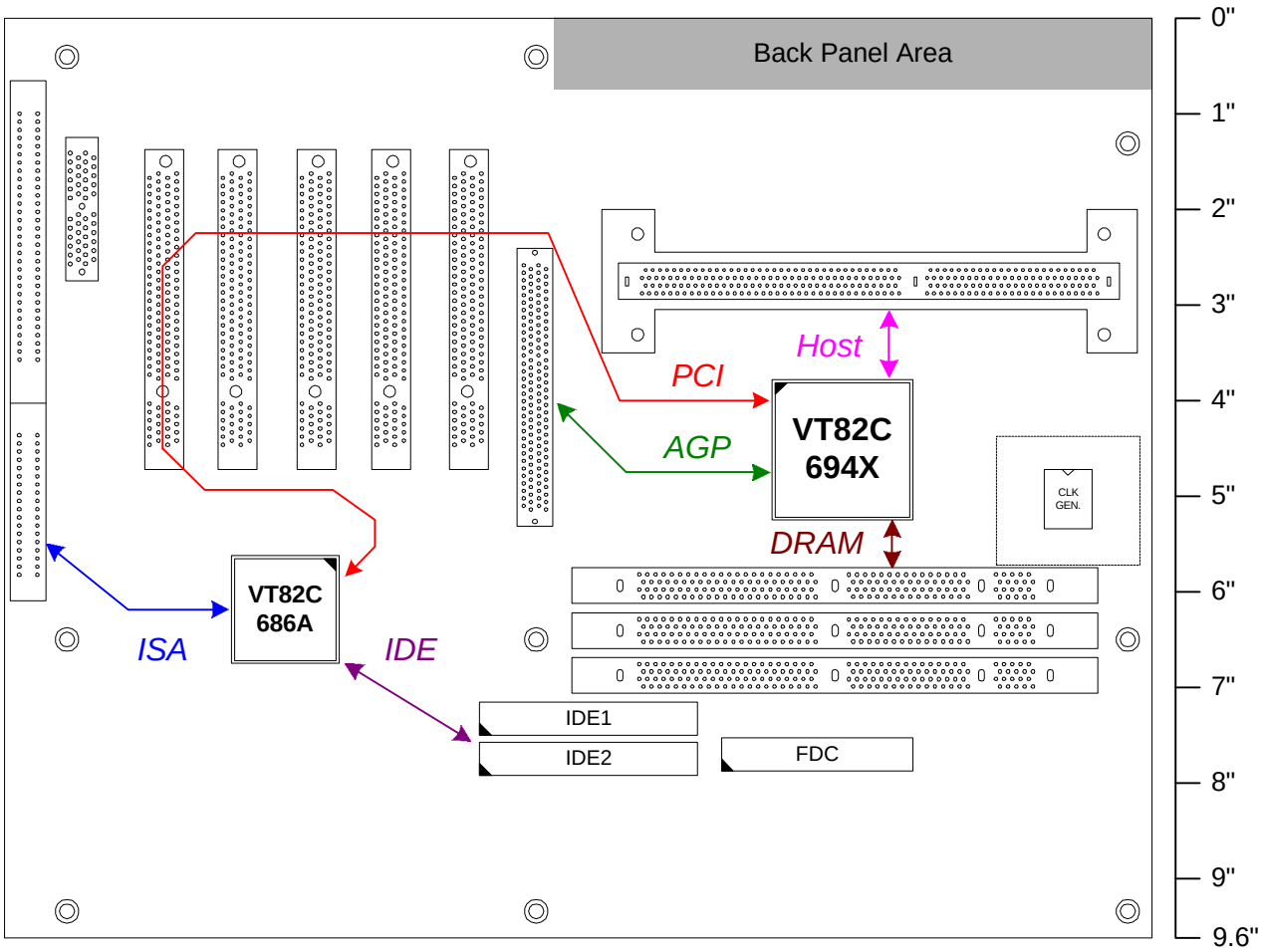


Figure 2-3. ATX Placement and Routing Example for Slot-1 System

2.2.1.2 Micro ATX Form Factor for Slot-1 System

A proposed component placement and signal group routings for an Apollo Pro133A micro-ATX system design is illustrated in Figure 2-4. The major components on the board are single Slot-1 CPU, two PCI slots, one AMR, one ISA slot and two DIMM slots. This figure shows a reference only micro-ATX motherboard placement. The placement should be re-evaluated if a different combination of AGP, PCI and ISA slots and other motherboard peripherals is desired.

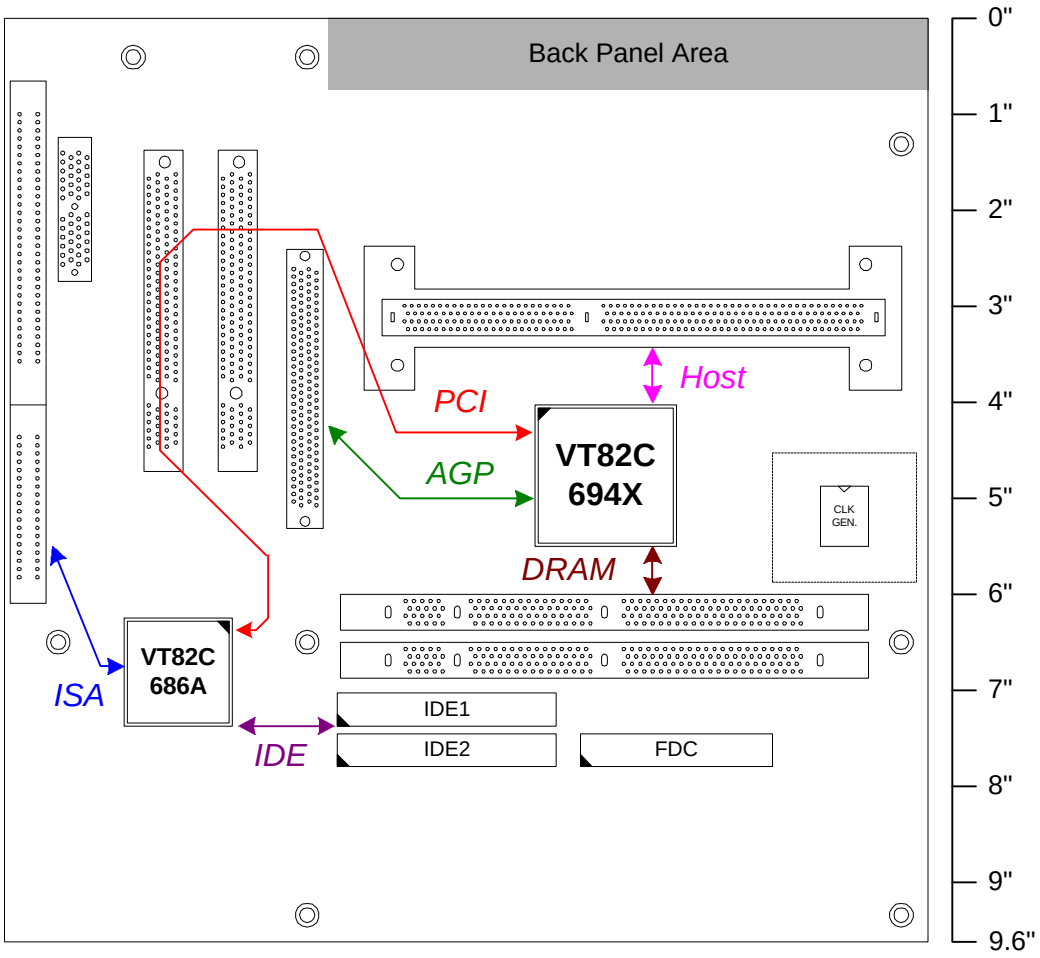


Figure 2-4. Micro-ATX Placement and Routing Example for Slot-1 System

2.2.2 Socket-370 Motherboard Placement and Routing

For Socket-370 CPU and Apollo Pro133A PC motherboard designs, two proposed placements and group signal routings for the two most popular form factors (ATX and micro-ATX) are shown in figures 2-5 and 2-6 respectively. Detailed layout guidelines and signal routings for the Pro133A chipset will be addressed later in section 2.4.

Each figure shows a full size of its respective form factor. The empty area at the bottom of each placement diagram can be eliminated to reduce the board size. Table 2-2 shows the full size and the suggested compact size for each form factor implementation.

Table 2-2. Different Board Size Lists for Socket-370 System

Form Factor Type	Full size	Compact Size	Specification
ATX	12" x 9.6" (30.5cm x 24.5cm)	12" x 8.3" (30.5cm x 21cm)	1 AGP, 5 PCI, 1 AMR, 1 ISA, 3 DIMM
Micro-ATX	9.6" x 9.6" (24.5cm x 24.5cm)	9.6" x 8.3" (24.5cm x 21cm)	1 AGP, 2 PCI, 1 AMR, 1 ISA, 2 DIMM

2.2.2.1 ATX Form Factor for Socket-370 System

A proposed component placement and signal group routing for an Apollo Pro133A ATX form factor system design is illustrated in Figure 2-5. The major components on the board are single Socket-370 CPU, five PCI slots, one AMR, one ISA slot and three DIMM slots. This figure shows an ATX motherboard placement as a reference only. The placement should be re-evaluated if a different combination of AGP, PCI and ISA slots and other motherboard peripherals is desired.

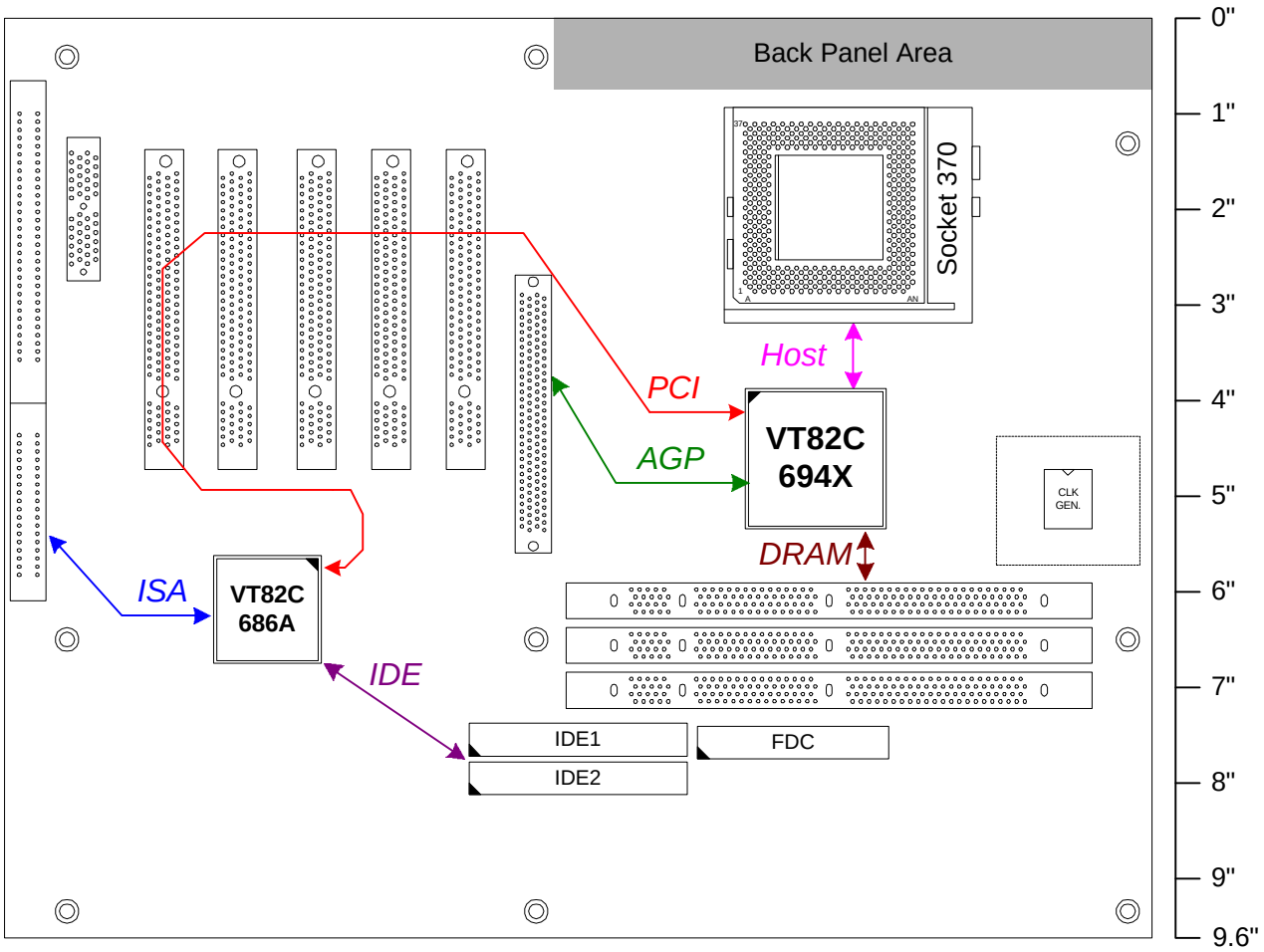


Figure 2-5. ATX Placement and Routing Example for Socket-370 System

2.2.2.2 Micro ATX Form Factor for Socket-370 System

A proposed component placement and signal group routing for an Apollo Pro133A micro-ATX system design is illustrated in Figure 2-6. The major components on the board are single Socket-370 CPU, two PCI slots, one AMR, one ISA slot and two DIMM slots. This figure shows a reference only micro-ATX motherboard placement. The placement should be re-evaluated if a different combination of AGP, PCI and ISA slots and other motherboard peripherals is desired.

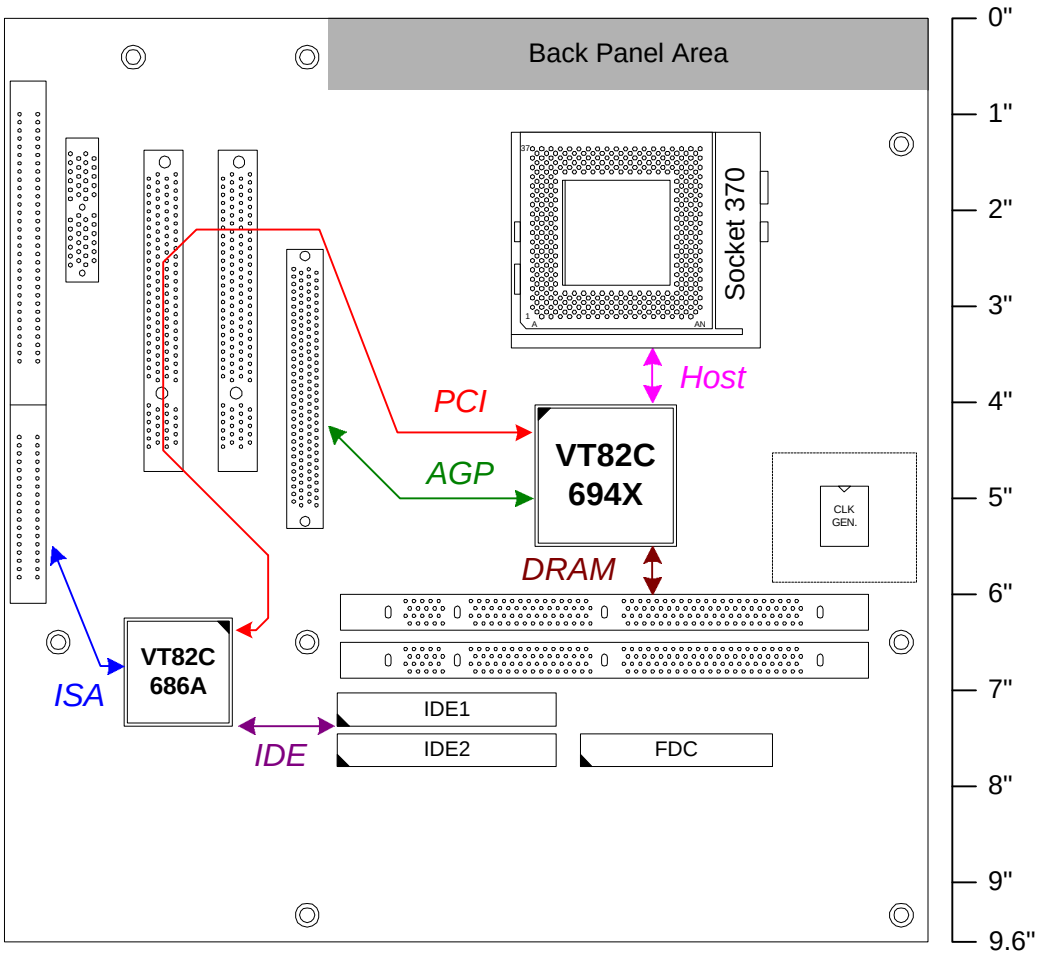


Figure 2-6. Micro-ATX Placement and Routing Example for Socket-370 System

2.2.3 Printed Circuit Board Description

A brief description of the Printed Circuit Board (PCB) for an Apollo Pro133A based system is provided in this section. From a cost-effectiveness point of view, a four-layer board is recommended for the motherboard design. For better quality, a six-layer board is preferred. These two types of boards will be discussed below:

2.2.3.1 Four-Layer Board

A four-layer stack-up with 2 signal layers and 2 power planes is shown in Figure 2-7. The two signal layers are referred to as the component layer and the solder layer. The two power planes are the power layer and the ground layer. The sequence of component layer-ground layer-power layer-solder layer is the most common stack-up arrangement from top to bottom. It is recommended to place a 5~6 mil substrate between the solder layer and the power plane and between the component layer and the ground plane, with a 42~45 mil substrate between the power and ground planes. Dielectric constant, E_r, should be 4.5 for all substrate materials.

Routing any signal trace on the power planes, either on the power layer or on the ground layer, is not recommended. If a signal must be routed on the power planes, then it should be routed as short as possible on the power layer, not on the ground layer. The impedance of all signal layers is to be in the range between 55 ohms and 75 ohms. Lower trace impedance providing better signal quality is preferred over higher trace impedance for clock signals.

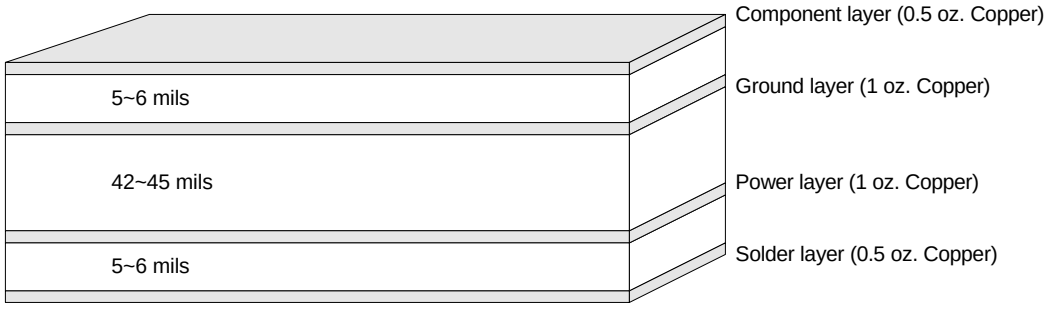


Figure 2-7. Four-Layer Stack-up with 2 Signal Layers and 2 Power Planes

2.2.3.2 Six-Layer Board

Figure 2-8 illustrates an example of a six-layer stack-up with 4 signal layers and 2 power planes. The layer sequence of component-ground-internal1-internal2-power-solder is the most common stack-up arrangement from top to bottom. It is recommended to place a 5~6 mil substrate between the signal layer and the power plane and place 30~35 mil substrate between two internal layers. A 7-mil substrate must be placed between the power plane and the internal layer. Dielectric constant, E_r, should be 4.5 for all substrate materials.

In order to reduce crosstalk effects between layers, signal traces on the two internal layers should be orthogonal. Routing any signal trace on the power planes, either on the power layer or on the ground layer, is also not recommended on a six-layer board. As an exception, if a signal has been routed on the power layer, then it should be routed as short as possible. In any case, routing on the ground layer is not allowed. The impedance of all signal layers is to be in the range between 55 ohms and 75 ohms. Lower trace impedance providing better signal quality is preferred over higher trace impedance for clock signals.

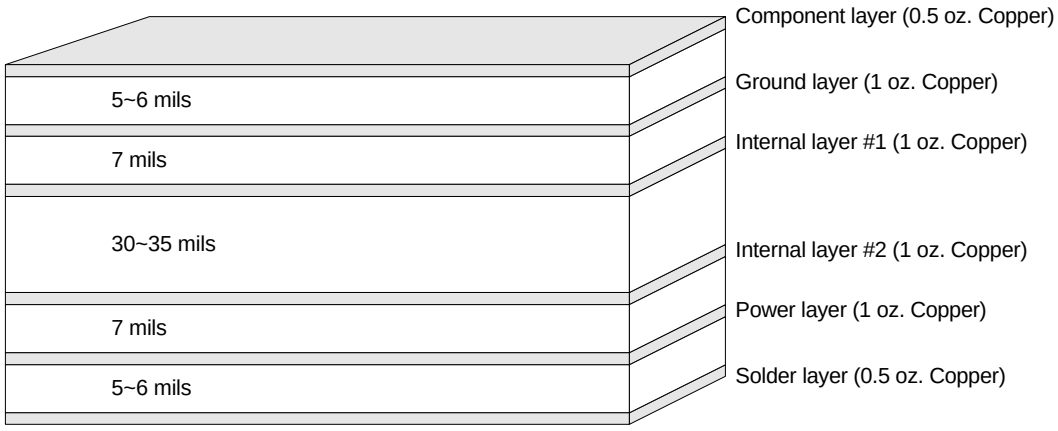


Figure 2-8. Six-Layer Stack-up with 4 Signal Layers and 2 Power Planes

2.2.4 On Board Power Regulation

Currently, the voltage range of the Slot-1 processor core voltage (VCC_CORE) is between 2.1V and 3.3V. And the voltage range of the Socket-370 processor core voltage is between 1.3V to 2.05V. Local regulation of VCC_CORE is recommended. That is, a local DC-to-DC converter, placed as close to the CPU as possible, converts a higher voltage to a lower voltage using a linear or switching (preferred) regulator. Bulk decoupling capacitors (greater than 10uF, Electrolytic or Tantalum) are used to prevent power supply droop. The closer to the load the capacitor is placed, the more inductance is bypassed.

2.2.5 Capacitive Decoupling

This section describes issues related to the capacitive decoupling of a Slot-1 CPU, Socket-370 CPU, Apollo Pro133A chipsets and DRAM Modules. It is well known that appropriate decoupling capacitors are required to provide a stable power source to the CPU, the ASIC and all other components on a motherboard. Moreover, details about capacitor type and placement on a motherboard are also given.

Decoupling capacitors are required to provide a stable power source to a CPU on a motherboard. Usually, low ESR and low ESL capacitors are preferred for decoupling. High frequency decoupling capacitors (less than 10uF, ceramic) are used to provide adequate decouplings. For example, 0.1uF, 1uF and 4.7uF capacitors can be treated as high frequency decoupling capacitors. It is recommended to keep vias for decoupling capacitors (SMD type) as close to the capacitor pads as possible (see Figure 2-9).

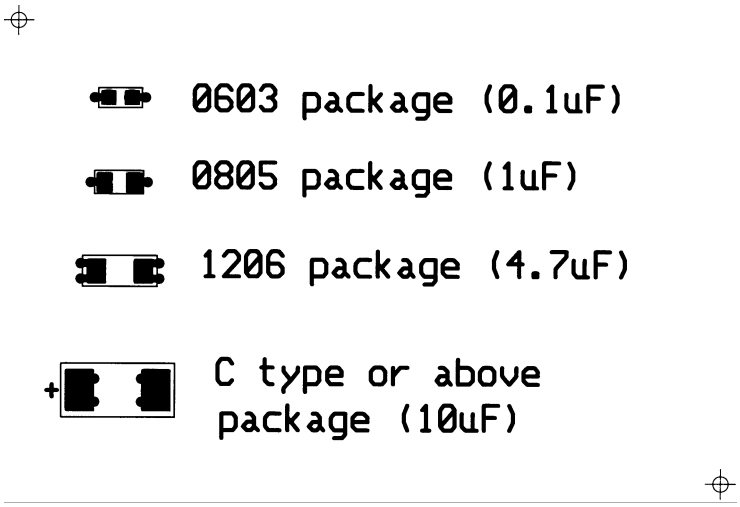


Figure 2-9. Example of Via Location

2.2.5.1 Single Slot-1 Processor Capacitive Decoupling

Figure 2-10 shows a suggested decoupling capacitor placement for the Slot-1 CPU. The isolation region between any two of the VCC_CORE (Core voltage 2.1V~3.3V) island, the VCC3 (I/O voltage 3.3V) island, the VTT (GTL+ termination voltage 1.5V) island and the VCC5 (5V) should be at least 30 mil wide. An island can be an entire power plane or a portion of a power plane that has been divided. The high frequency decoupling capacitors (0.1uF and 1.0uF) should be located as close to the power and ground pins of the Slot-1 as possible.

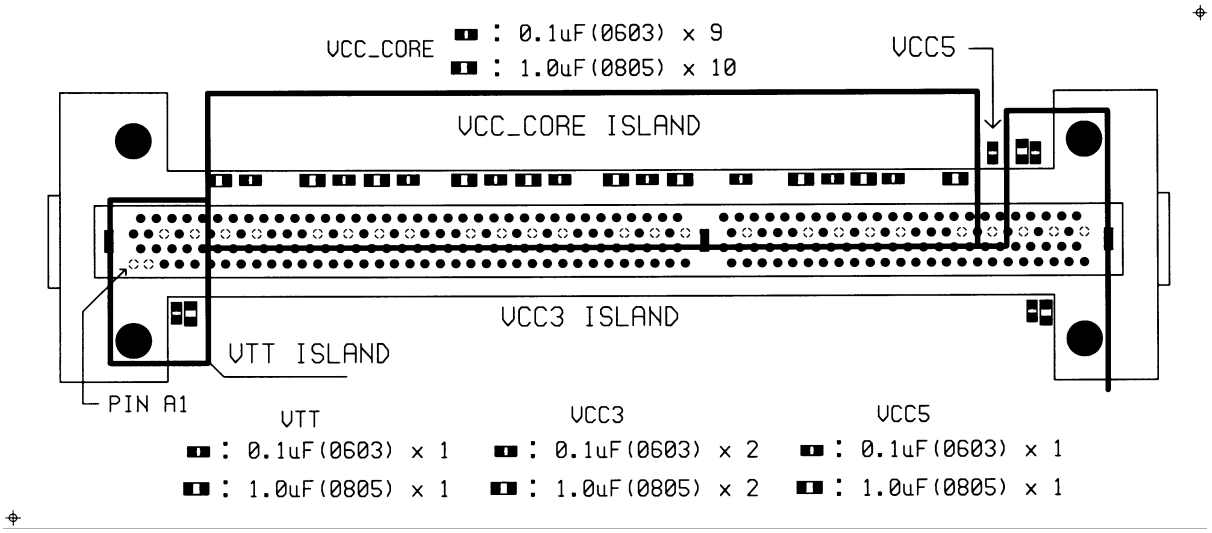


Figure 2-10. Decoupling Capacitor Placement for Single Slot-1 Processor

Notes:

1. The white round dot represents the power pin of the specified power island. For example, there are four VTT power pins on the VTT island. (Slot-1 CPU power pins: VCC_CORE x 19, VTT x 4, VCC3 x 3 and VCC5 x 1)

2. Recommended numbers of the decoupling capacitors for each power plane are shown in Figure 2-10.

2.2.5.2 Single Socket-370 Processor Capacitive Decoupling

A suggested decoupling capacitor placement for the Socket-370 CPU is shown in Figure 2-11. The high frequency decoupling capacitors (0.1uF and 1uF) should be located as close to the power and ground pins of the Socket-370 as possible. One hundred and twelve 56 ohm termination resistors are required for the GTL+ bus (HD[63:0], HA[31:3] and 19 host control signals) on the motherboard. There are at least 28 R-packs (4 resistors for a discrete R-pack) for the VTT termination. It is recommended to place one 1uF decoupling capacitor for each two R-packs. There are also four 1000uF capacitors for GTL+ termination voltage (VTT) located at the four corners of the Socket-370 in Figure 2-11. Most of the high frequency decoupling capacitors are located in Socket-370 cavity. The recommended distribution of these high frequency and bulk decoupling capacitors for various voltage power pins is listed in Table 2-3.

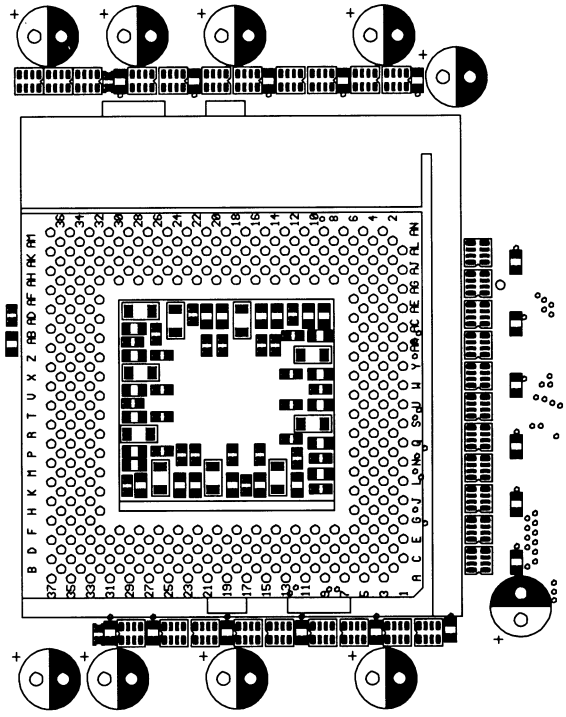


Figure 2-11. Decoupling Capacitor Placement for Single Socket-370 Processor

Table 2-3. High Frequency and Bulk Decoupling Capacitor Distribution around Socket-370

Power Pin Name	Voltage Level	Decoupling & Bulk Capacitor	Location
VCORE x **59** (CPU Core Voltage)	2.0V or 1.55V (future)	4.7uF x 10, 1uF x 23, 0.1uF x 21	Socket-370 inner block
		1000uF x 6 (4 for switching regular)	3 at upper middle and 3 at lower middle
VREF x **8** (GTL+ Reference Voltage)	1.0V (2/3 VCC15)	0.1uF x 6	Socket-370 inner block
		1uF x 1, 0.1uF x 1	Around Socket-370
VCC15 x **1** (GTL+ Termination Voltage)	1.5V	1uF x 1	Around Socket-370
		1000uF x 4	Four corners of the Socket-370
VCCCMOS x **1** (CMOS Interface Voltage)	2.5V or 1.5V(future)	1uF x 1	Around Socket-370
VCC25 x **1**	2.5V	1uF x 1	Around Socket-370

2.2.5.3 Apollo Pro133A Chipset Capacitive Decoupling

Decoupling capacitors for the VT82C694X and VT82C686A are shown in Figure 2-12. It is recommended to place decoupling capacitors as close to the chips as possible and evenly distribute these capacitors around them. In most cases, the value of these decoupling capacitors is 1uF, but 0.1uF capacitors are also acceptable. Similarly, this kind of placement can apply on other ASIC chips, slots or sockets.

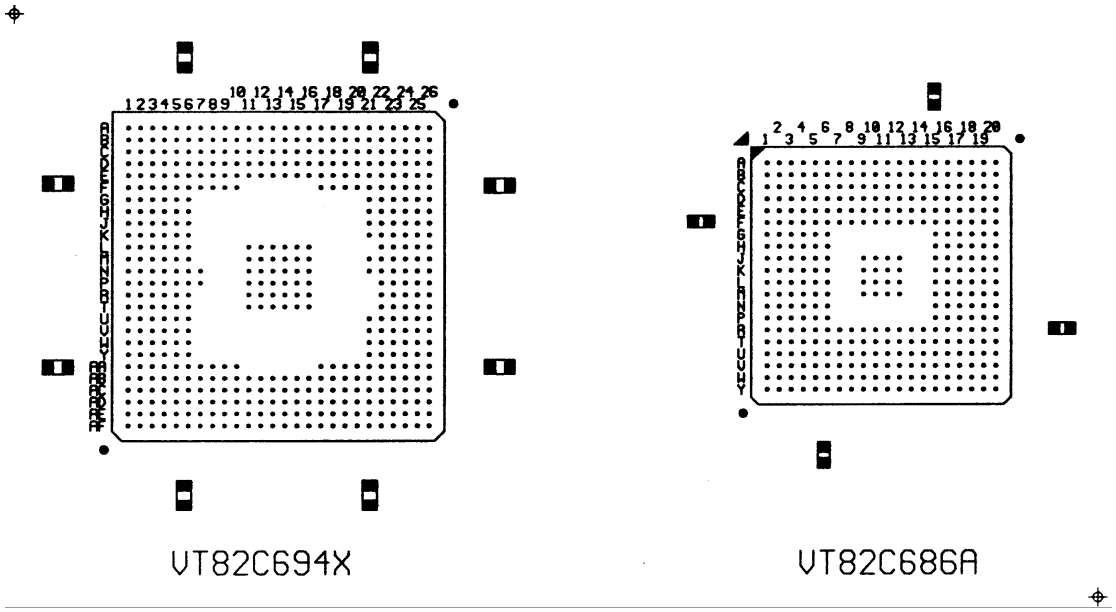


Figure 2-12. Decoupling Capacitor Placements for VT82C694X and VT82C686A

2.2.5.4 DRAM Module Capacitive Decoupling

The capacitive decoupling for SDRAM modules should be taken good care of since SDRAM modules running at 133MHz clock consume much more power (about 1.76A for each double side DIMM module at maximum). Figure 2-13 shows a placement example for SDRAM module decoupling.

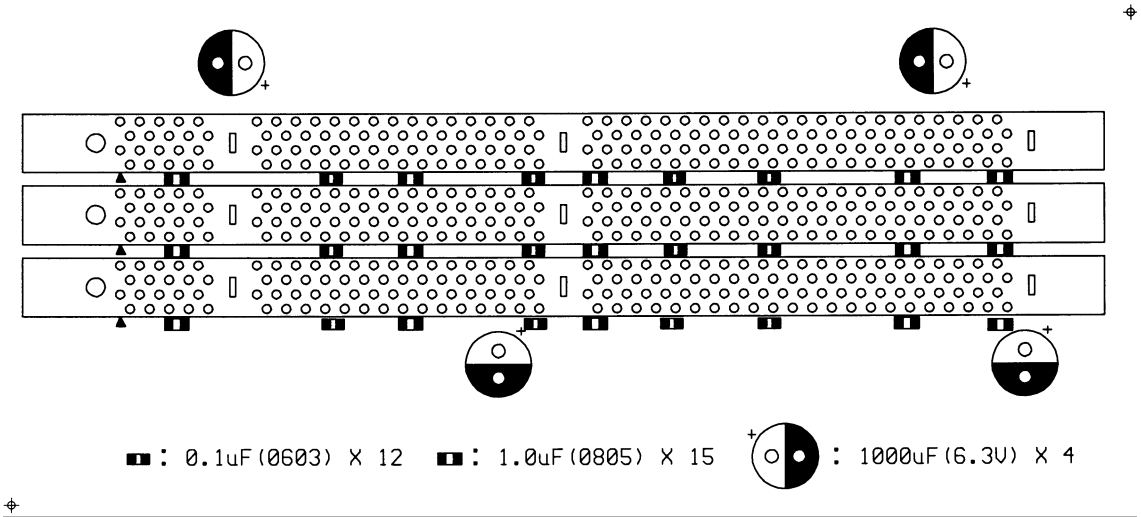


Figure 2-13. Decoupling Capacitor Placements for DRAM Modules

Note: *North Bridge controller (VT82C694X) is located at the north side of these DIMM Slots.*

2.2.6 Power Plane Partitions

The required voltage sources in an Apollo Pro133A system design are: +/-12V, +/-5V, CPU core voltage (1.3V~3.3V defined by the five voltage identification pins of the Slot-1 or Socket-370 CPU), 3.3V, 2.5V and 1.5V. The power layer is partitioned into several power islands with five major power sources: **VCC_CORE** (CPU core voltage), **VCC3** (3.3V), **VTT** (1.5V GTL+ termination voltage), **VDDQ** (3.3V for AGP 2X mode or 1.5V for AGP 4X mode) and **VCC5** (+5V). The remaining power sources will have their own small power islands or be routed as power traces 20-50 mils wide.

2.2.6.1 Power Plane Partitions for Slot-1 Motherboard

Figure 2-14 shows the power plane partitions on a typical ATX form factor. The island associated with VCC_CORE covers almost half the area of the Pentium-II socket for the Slot-1 CPU. The VCC3 island covers an area, which contains the North Bridge chip, the South Bridge chip, all DIMM slots and a half of the AGP slot. The VDDQ island occupies most AGP signal routing area. The rest of the power layer belongs to VCC5. Different power plane partitions for Micro-ATX form factor are shown in Figure 2-15. The distribution of power islands is almost the same between ATX and Micro-ATX, except the smaller VCC5 island on the power layer of the Micro-ATX.

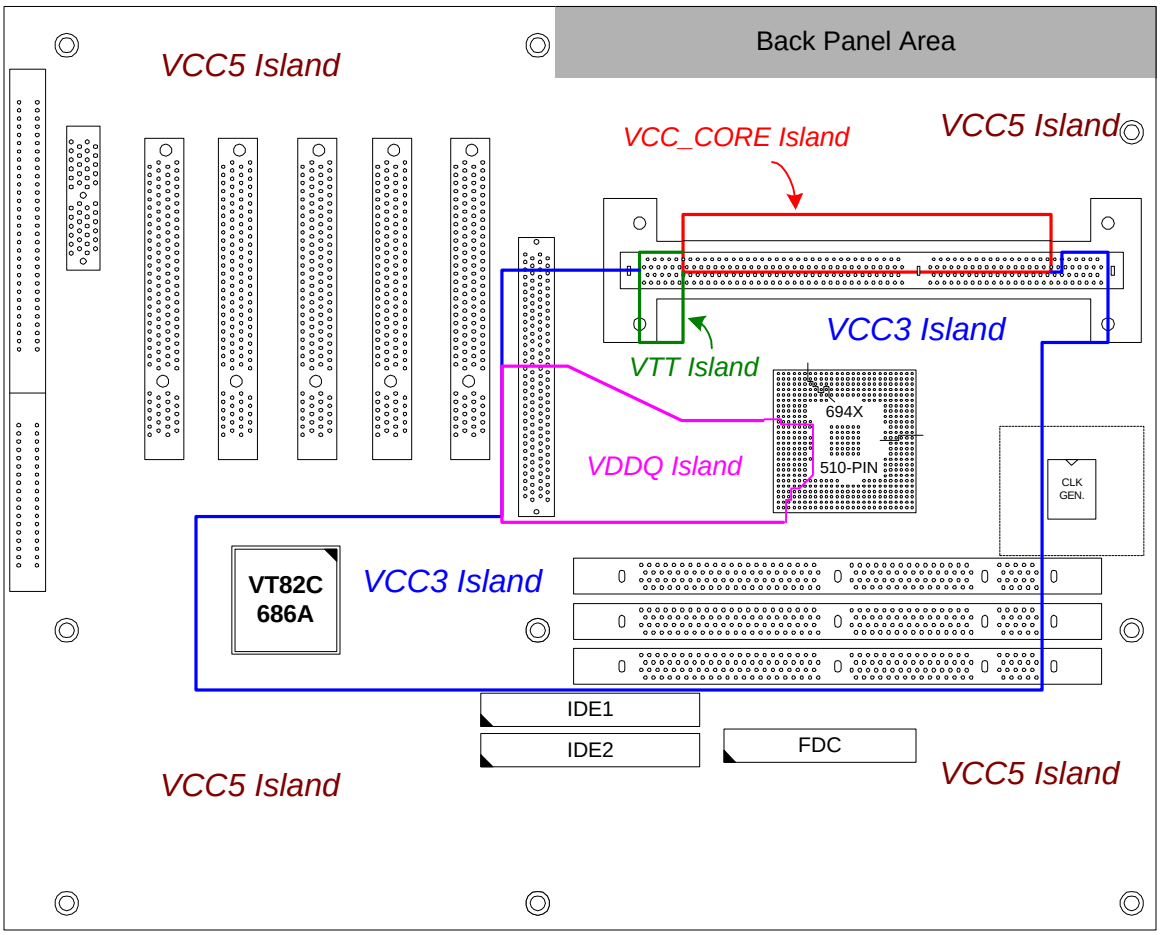


Figure 2-14. ATX Power Plane Partitions for Slot-1 System

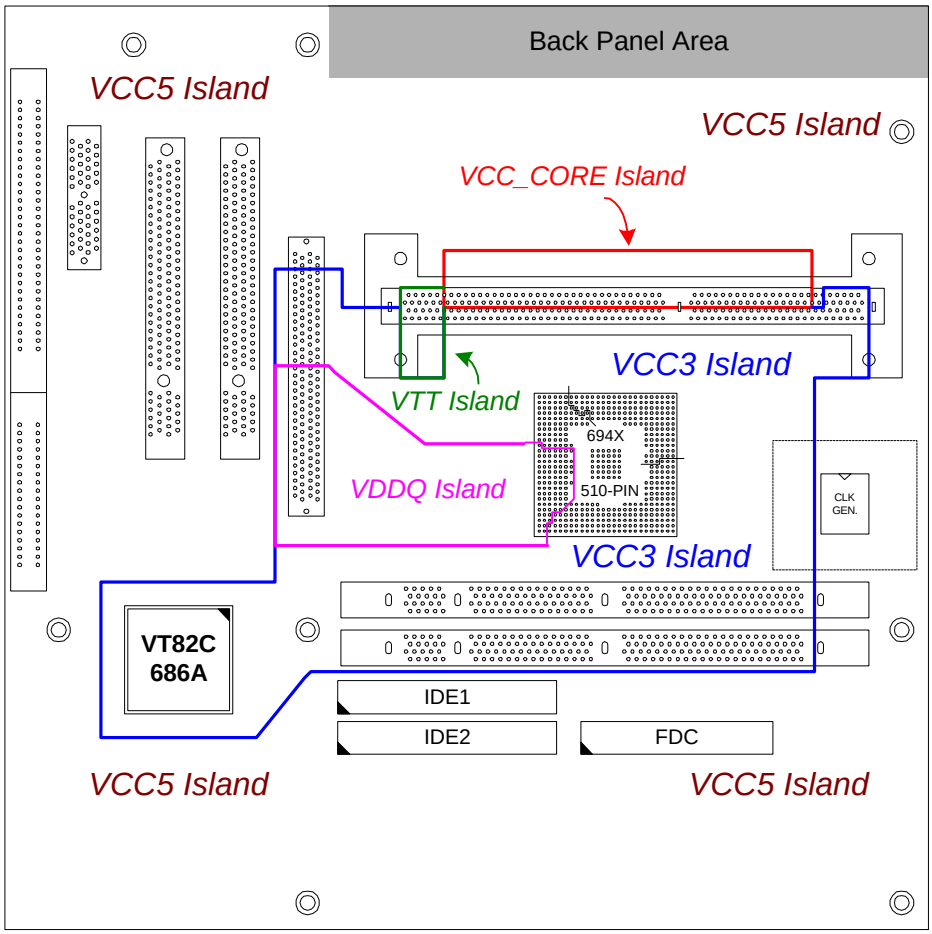


Figure 2-15. Micro-ATX Power Plane Partitions for Slot-1 System

2.2.6.2 Power Plane Partitions for Socket-370 Motherboard

Figure 2-16 shows the power plane partitions on a typical ATX form factor. The island associated with VCC_CORE covers the whole area of the PPGA socket for the Socket-370 CPU. The VCC3 island covers an area that contains the North Bridge chip, the South Bridge chip, all DIMM slots and a half of the AGP slot. The VDDQ island occupies most AGP signal routing area. The rest of the power layer belongs to VCC5. Different power plane partitions for Micro-ATX form factor are shown in Figure 2-17. The distribution of power islands is almost the same between ATX and Micro-ATX, except the smaller VCC5 island on the power layer of the Micro-ATX.

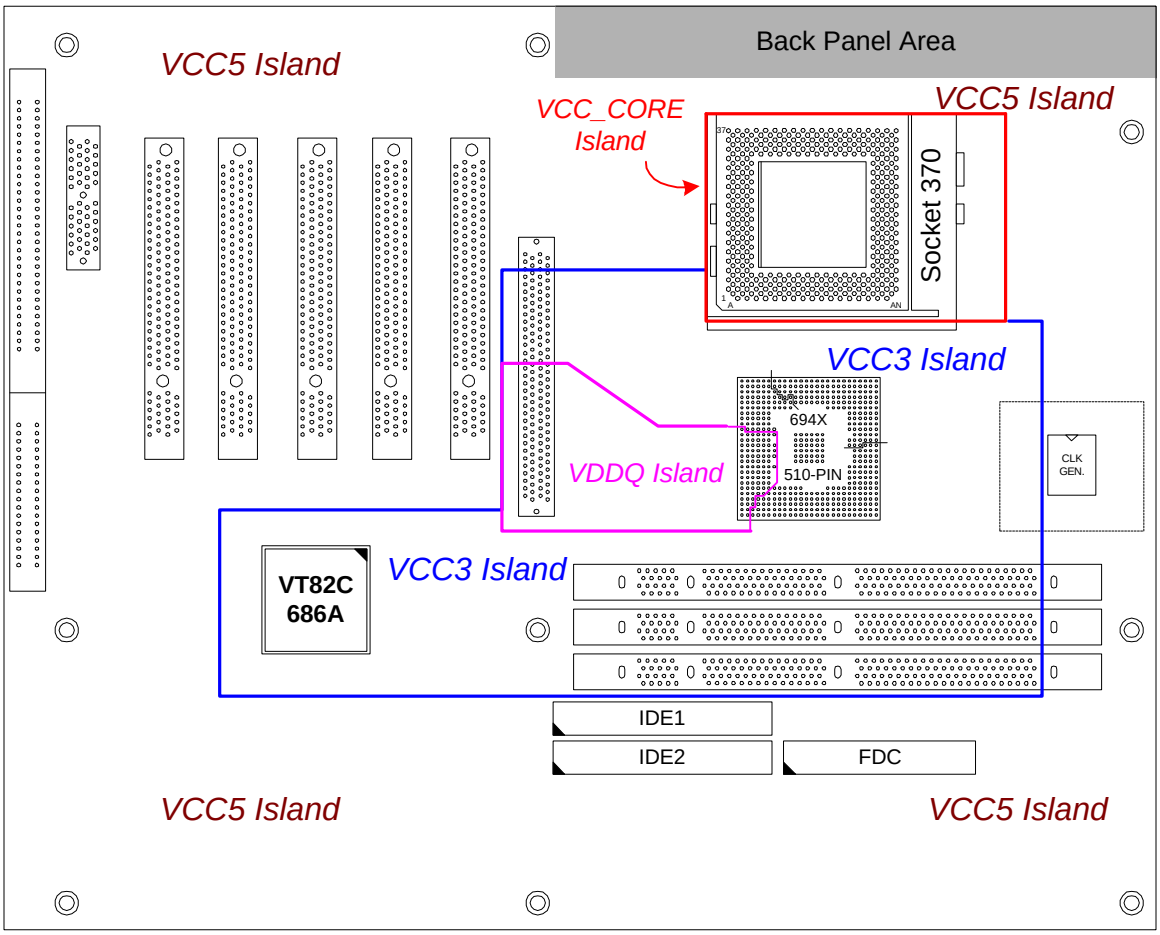


Figure 2-16. ATX Power Plane Partitions for Socket-370 System

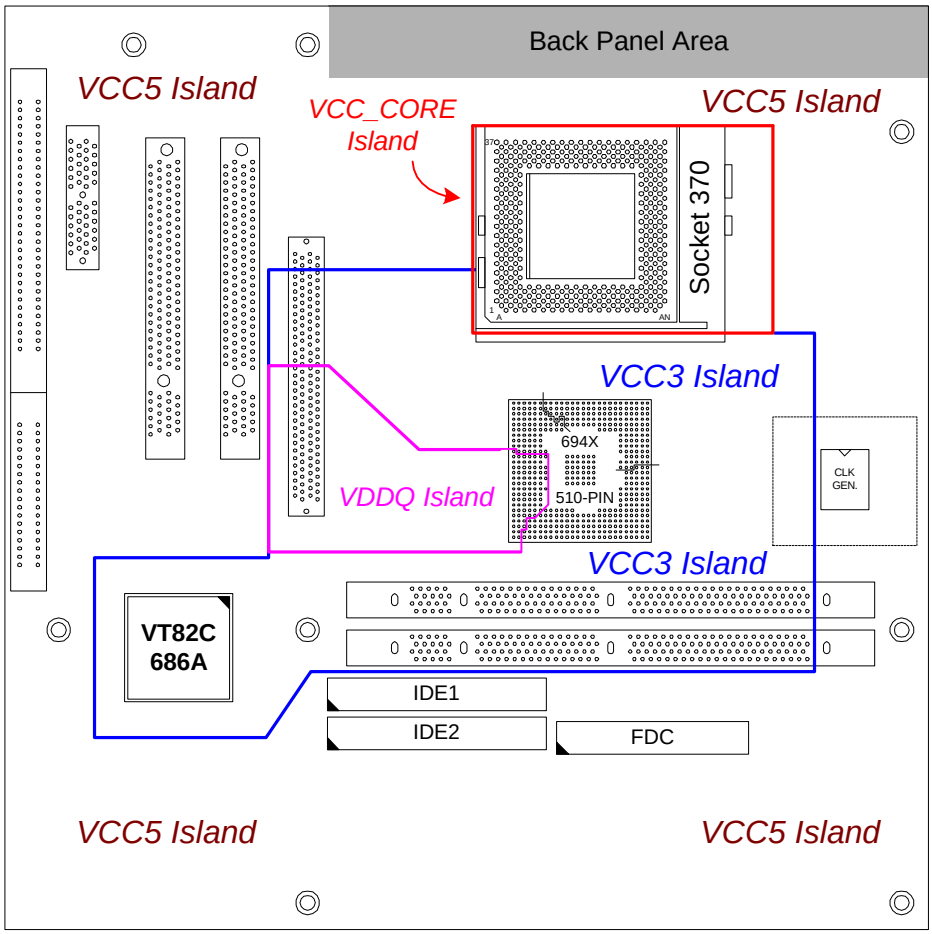
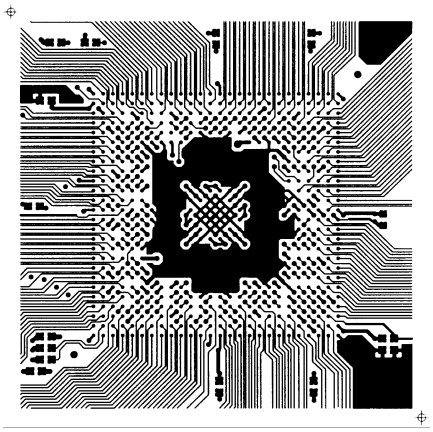


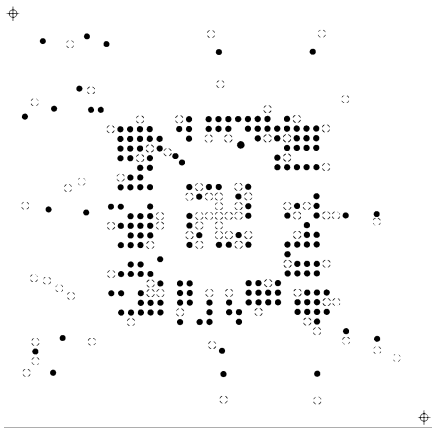
Figure 2-17. Micro-ATX Power Plane Partitions for Socket-370 System

2.2.7 Chipset Power and Ground Layout Recommendations

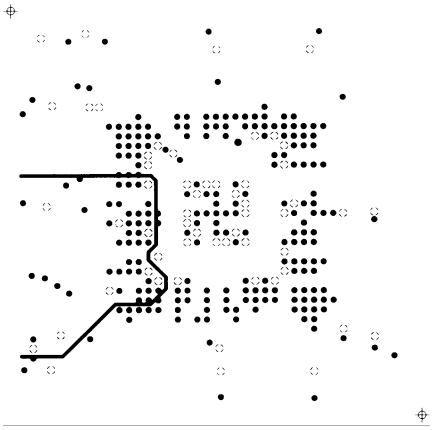
This section shows the recommended layout of the power plane and the ground plane on each layer for the two VIA BGA chips (VT82C694X and VT82C686A). Appropriate power and ground distributions for component, ground, power and solder layers can provide a better power and ground circuit to the chip. Two examples of power and ground layout and signal routings for both VT82C694X and VT82C686A are shown in Figures 2-18 and 2-19 respectively.



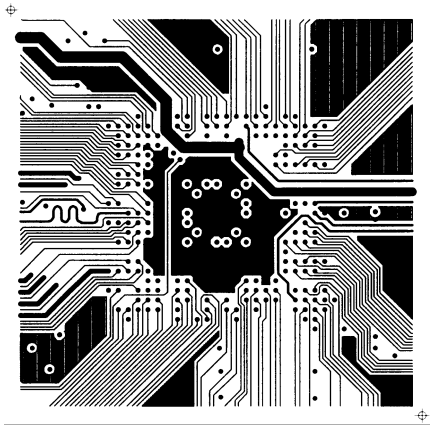
(a) Component Layer



(b) Ground Layer



(c) Power Layer

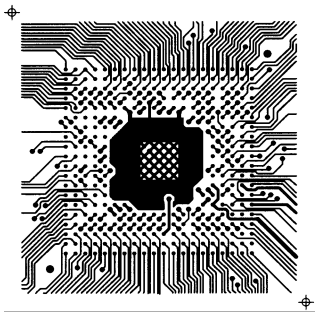


(d) Solder Layer

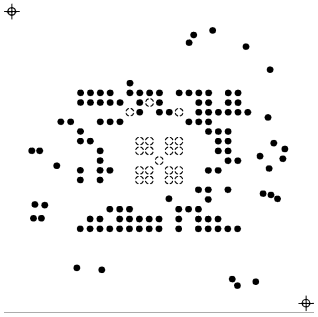
Figure 2-18. VT82C694X Power and Ground Layout

Notes:

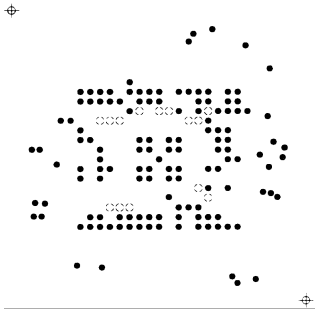
1. *In Figure 2-18 (b) and (c), a black round dot represents a via with no connection to the specified layer and a white round dot represents a via with a connection to the specified layer. For example, the white round dots in Figure 2-18 (b) are ground connection vias and the white round dots in Figure 2-18 (c) can be VDDQ or VCC3 connection vias.*
2. *The square-like rail in the center area of the VT82C694X chip on the component layer in Figure 2-18 (a) connects to ground. The center square-like block representing an unused routing area connects to ground in Figure 2-18 (d).*
3. *Pin A1 of the VT82C694X chip is located at the upper-left corner.*
4. *The left area surrounded by the isolation (black line) is the AGP VDDQ power plane in Figure 2-18 (c).*



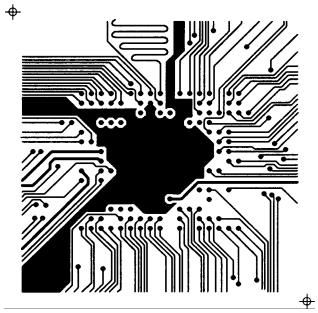
(a) Component Layer



(b) Ground Layer



(c) Power Layer



(d) Solder Layer

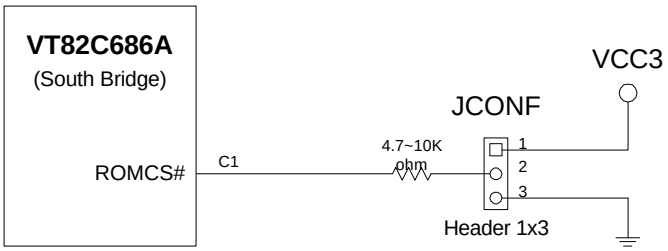
Figure 2-19. VT82C686A Power and Ground Layout

Notes:

1. *In Figure 2-19 (b) and (c), a black round dot represents a via with no connection to the specified layer and a white round dot represents a via with a connection to the specified layer. For example, the white round dots in Figure 2-19 (b) are ground connection vias and the white round dots in Figure 2-19 (c) are VCC3 connection vias.*
2. *The square-like rail in the center area of the VT82C686A chip on the component layer in Figure 2-19 (a) connects to ground. The center square-like block representing an unused routing area connects to ground in Figure 2-19 (d).*
3. *Pin A1 of the VT82C686A chip is located at the upper-left corner.*

2.2.8 Power Up Configuration

During system restart and power up, system configuration information is latched at the rising edge of the RESET# signal. All signals used to select power-up strap options are connected to either internal pull-up or pull-down resistors of minimum 50K ohms (maximum is 150K ohm). These internal resistors select a default mode on the signal during reset. To enable different modes, external pull-ups or pull-downs (the opposite of the internal pull-up or pull-down) of approximately 10K ohm can be connected to particular signals. These pull-ups or pull-downs should be connected to the relative (e.g. 3.3V) power supply. For example, a 3-pin jumper is used to select a pull-up (1-2) or pull-down (2-3) strapping as shown in Figure 2-20. The strapping state of logical 1 or logical 0 can be selected by using a jumper (shortage between pins).



JCONF	CPU Configuration
1-2	Slot-1 or Socket-370
2-3	Socket-7

Figure 2-20. A Typical Example of a 3-pin Jumper Strapping Circuit

2.2.8.1 VT82C694X Power Up Strappings

Internal configuration registers of Apollo Pro133A digital core logic are based on the status of memory address lines (MAB[12:11]#, MAB10, MAB[9:6]#) and Host address lines (A15# and A7#). These memory address signals are pulled up or pulled down with internal resistors on their I/O buffers to determine the default configurations. If the default configuration setting is acceptable, no external pulled down resistors are necessary. However, the existence of an external pull-up or pull-down will insure that the correct configuration is detected. These memory address signals may be pulled up or pulled down with external resistors to determine the desired configurations. Please refer to Table 2-4 for the power up configuration of all strapping signals.

Table 2-4. Power-Up Configuration for VT82C694X

Signal Name	Pin #	Strapping Description	Note
MAB12#	AD21	CPU Bus Frequency Select: **0** = 66MHz, **1** = 100MHz	1,2
MAB11#	AE21	In Order Queue Depth (IOQD) Enable: **0** = Non-Pipelined, **1** = Maximum Queue Depth Enabled	1,2
MAB10	AB20	Quick Start Select (Mobile only): **0 =** Enable Standard Stop Clock Mode, **1** = Enable Quick Start Mode	1,2
MAB9#	AC20	AGP Enable: **0** = Enable AGP Function, **1** = Disable AGP Function	1,2
MAB8#	AF20	CPU Frequency Select 1: **0** = 66/100MHz, **1** = 133MHz	1,2
MAB7#	AB19	Memory Module Configuration:	1,2
MAB6#	AB18	Mobile Buffers Enable: **0** = Use Desktop Buffers, **1** = Use Mobile Buffers	1,2
A15#	E22	Quick Start Select (Mobile only): **0** = Enable Quick Start Mode, **1** = Enable Standard Stop Clock Mode	1,3
A7#	G24	IOQD Status: **0** = 1, **1** = IOQD set to Maximum	1,3

Notes:
1. *"**0**" represents the logical state is "low". An external or internal pull-down resistor is required. Conversely, "**1**" represents the logical state is "high". An external or internal pull-up resistor is required.*
2. *MAB11# is connected to an internal 100K ohm pull-up resistor. MAB12#, MAB10, MAB[9:6]# are connected to internal 100K ohm pull-down resistors.*
3. *The A15# and A7# are terminated on the CPU bus with GTL+ termination (pull-up resistors).*

2.2.8.2 VT82C686A Power Up Strappings

The power up configuration for the VT82C686A South Bridge is shown in Table 2-5 below. The strapping of SPKR (pin V5 of the VT82C686A) is sampled during reset to determine the usage of the Secondary Disk Data (SDD) pins. When connecting the SPKR signal to a speaker, the strapping circuit of SPKR is slightly different from the regular strapping circuit. Two application circuits for SPKR strapping are shown in Appendix A.

Table 2-5. Power-Up Configuration for VT82C686A

Signal Name	Pin #	Strapping Description	Note
SPKR	V5	Selection for Secondary IDE data bus or Audio/GAME function: 1 = Audio/GAME (Audio/Game uses SDD bus and SA[15:0] can also function as SDD bus). 0 = Secondary IDE data bus (Primary IDE and Secondary IDE have their own data buses).	1
ROMCS#	C1	Selection of Socket-7 configuration or Slot-1 configuration: 1 = Slot-1 for Pentium II or Socket-370 (also called “Socket-9”) for Celeron 0 = Socket-7	1

Note:
1. “ 0” represents the logical state is “low”. An external or internal pull-down resistor is required. Conversely, “ 1” represent the local state is “ high”. An external or internal pull-up resistor is required.

2.3 General Layout and Routing Guidelines

This section provides general layout rules and routing guidelines for designing Apollo Pro133A motherboards.

2.3.1 Trace Attribute Recommendations

For most signal traces on an Apollo Pro133A motherboard layout, 5-mil trace width and 10-mil spacing are advised. To reduce trace inductance, minimum power trace width is set at 30 mils. As a quick reference, recommended trace width and spacing for different trace types are listed in Table 2-6.

Table 2-6. Recommended Trace Width and Spacing

Trace Type	Trace Width (mils)	Spacing (mils)
Signal	5 or wider	10 or wider
Clock	15 or wider	15 or wider
Power	30 or wider	20 or wider

In high-speed bus design, general rules for minimizing crosswalk are listed below:

- Maximize the distance between traces. Maintain a minimum 10 mils space between traces wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Select a board stack-up that minimizes coupling between adjacent traces.
- The recommended motherboard impedance should be in the range of 65 ohm +/- 5 ohm.

2.3.2 Apollo Pro133A Clock Layout Recommendations

2.3.2.1 Clock Requirements

The requirements of the system clock synthesizer for an Apollo Pro133A based system design are listed in Table 2-7.

Table 2-7. Apollo Pro133A Clock Synthesizer Requirements

Clock Signal Type	Frequency (MHz)	Quantity	Connections
CPU Clock	66/75/83/95/ 100/124/133	3	Connect to CPU (1), Apollo Pro133A (1) and ITP Debug Port (1)
SDRAM Clock	66/100/133	17	Connect to four SDRAM slots (16) and Apollo Pro133A (1)
SDRAM Clock In	66/100/133	1	Connect to Apollo Pro133A (1)
PCI Clock	33	7	Connect to Apollo Pro133A (1), South Bridge (1), and PCI slots (5)
USB Clock	48	1	Connect to South Bridge (1)
Super I/O Clock	24	1	Connect to Super I/O (1) if an external Super I/O is used
IOAPIC Clock	14.31818	1	Connect to Slot-1 or Socket-370 CPU
Reference Clock	14.31818	2	Connect to South Bridge (1) and ISA slots (1)

Note: The voltage level for CPU and IOAPIC clock signals is 2.5V. The voltage level for the remaining clocks is 3.3V.

Figure 2-21 shows clock connections of the system clock synthesizers to their respective destinations.

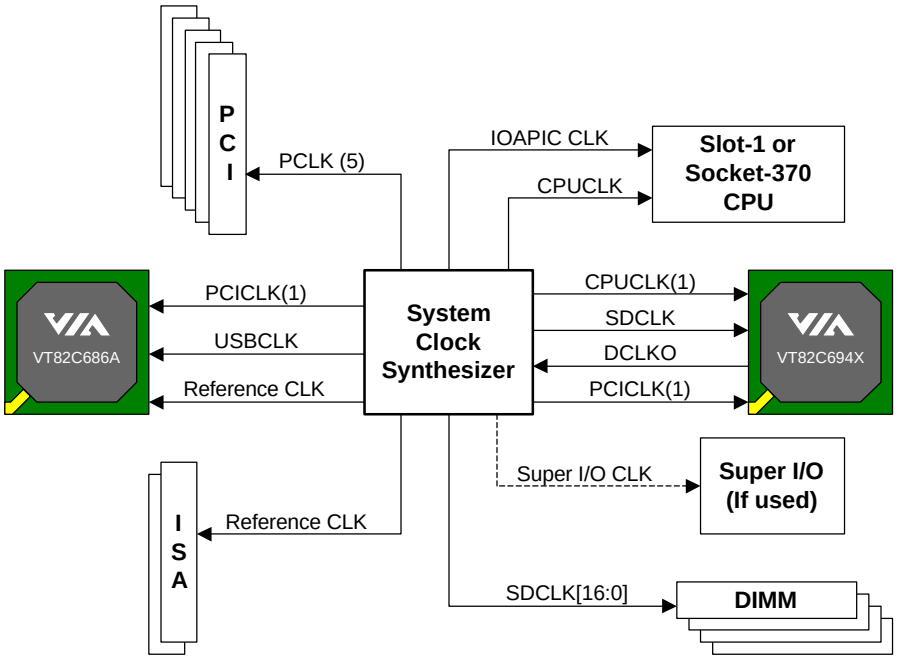


Figure 2-21. System Clock Connections

2.3.2.2 Clocking Scheme

The 17 (66 / 100 / 133MHz) SDRAM clocks are generated from a clock buffer inside the system clock synthesizer. They are controlled by the SDRAM clock output (DCLKO) provided by the Apollo Pro133A North Bridge. The VT82C694X (North Bridge) has a built-in de-skew Phase Lock Loop (PLL) circuitry for optimal skew control within and between clocking regions. For more details, refer to Figure 2-22.

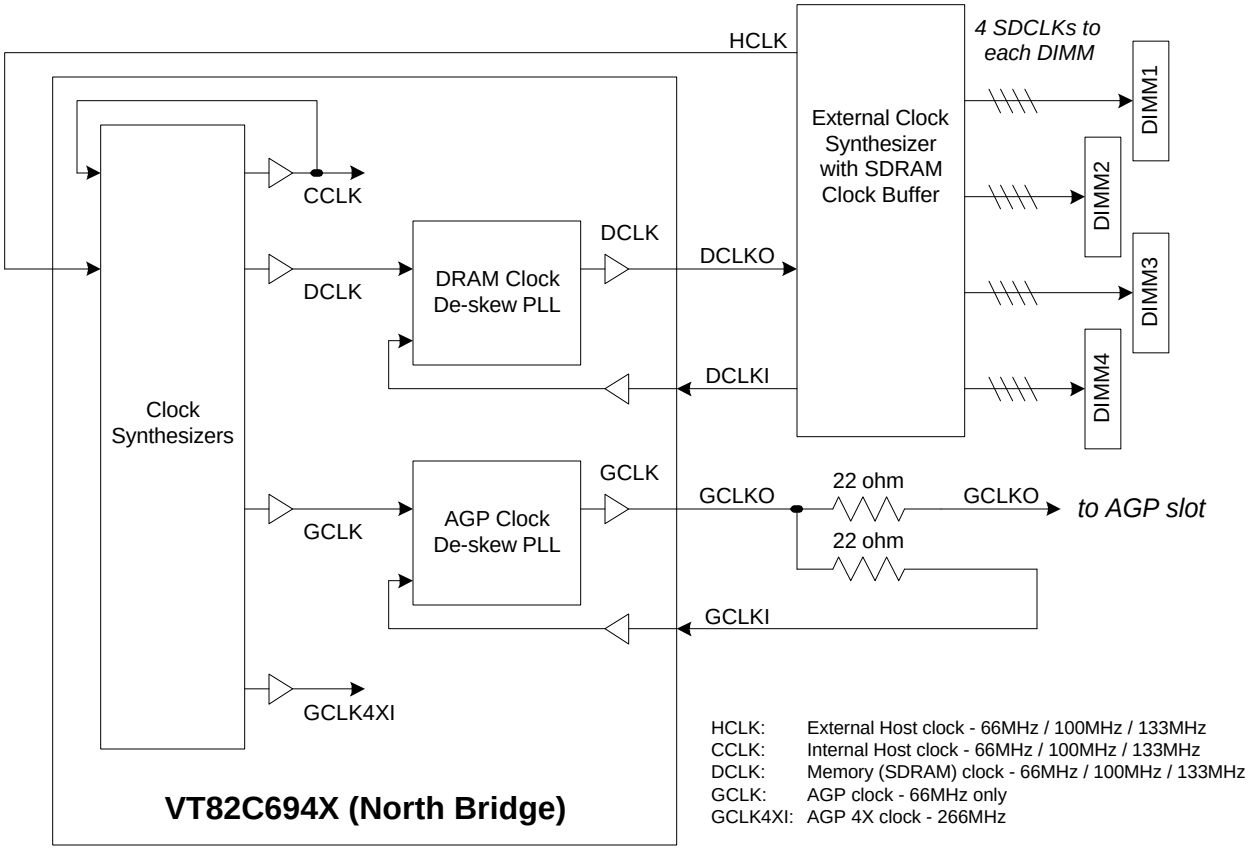


Figure 2-22. Apollo Pro133A Chip Clocking Scheme

2.3.2.3 Clock Routing Considerations

Clock routing guidelines are listed below:

- The recommended range of a clock trace width is between 15 mils and 20 mils.
- The minimum space between one clock trace and adjacent clock traces is 15 mils. The minimum space from one segment of a clock trace to other segments of the same clock trace is two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling (see Figure 2-23).
- Clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane (see Figure 2-24).
- Series terminations (damping resistors) are needed for all clock signals (typically 10 ohms to 33 ohms). When two loads are driven by one clock signal, the series termination layout is shown in Figure 2-25. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20 mils to 50 mils) are preferred.
- No clock traces on the internal layer if a six-layer board is used.

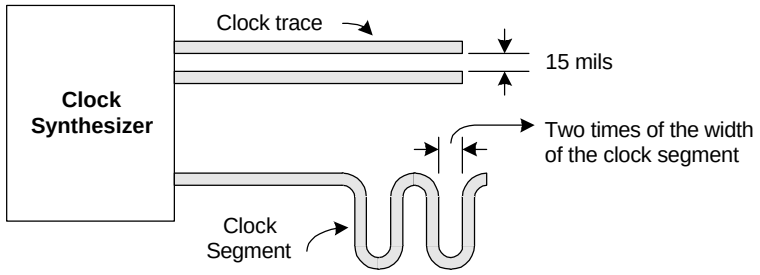


Figure 2-23. Clock Trace Spacing Guidelines

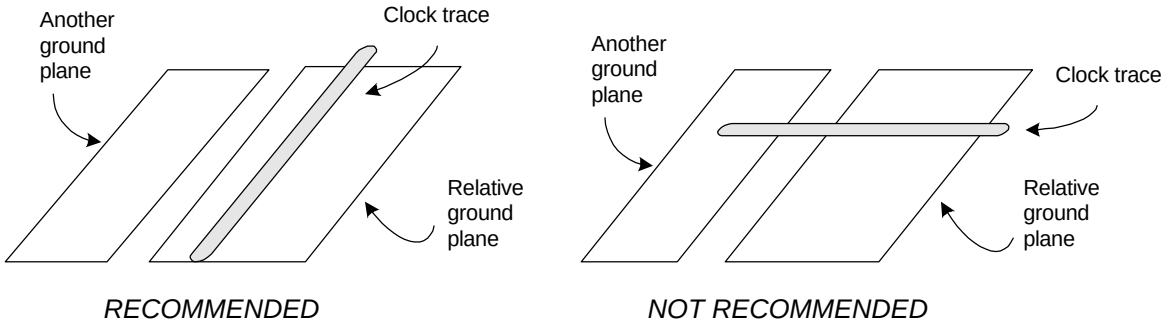


Figure 2-24. Effect of Ground Plane to a Clock Signal

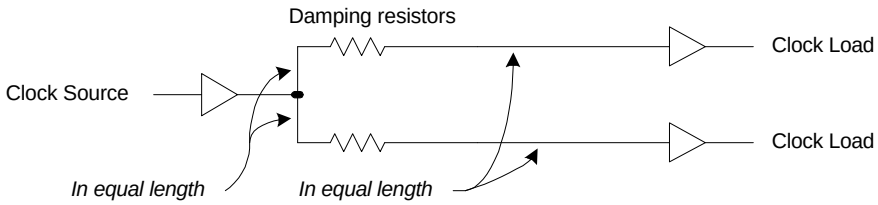


Figure 2-25. Series Termination for Multiple Clock Loads

2.3.2.4 System Clock Combinations

The major clock combinations for an Apollo Pro133A based system are listed in Table 8. Clock frequencies for the AGP clock and PCI clock are 66MHz and 33MHz respectively. Various clock combinations for the CPU clock and the SDRAM clock are determined by power-up strap options on MAB12# and MAB8#.

Table 2-8. Apollo Pro133A System Clock Combinations

CPU CLOCK	SDRAM CLOCK	AGP CLOCK	PCI CLOCK	CPU/PCI RATIO
133 MHz	133 MHz	66 MHz	33 MHz	4
	100 MHz	66 MHz	33 MHz	4
100 MHz	133 MHz	66 MHz	33 MHz	3
	100 MHz	66 MHz	33 MHz	3
	66 MHz	66 MHz	33 MHz	3
66 MHz	100 MHz	66 MHz	33 MHz	2
	66 MHz	66 MHz	33 MHz	2

2.3.2.5 Host CPU Clock and SDRAM Clock Signals

Layout recommendations for host clocks and SDRAM clocks for Slot-1 and Socket-370 CPUs are shown in Figure 2-26 and 2-27 respectively. 22 ohm and 10 ohm series terminations are recommended for all host clocks and all SDRAM clocks respectively. It is also recommended that bypass capacitors be added to all clock signals on the clock synthesizer side. Different values of series terminations and bypass capacitors are needed for a better clock transmission and alignment on the final PCB layout. In other words, it is best to observe the actual clock waveform and experimentally determine the optimal values for series termination and bypass capacitors. For clock alignment considerations, trace lengths of all clocks should match the longest one.

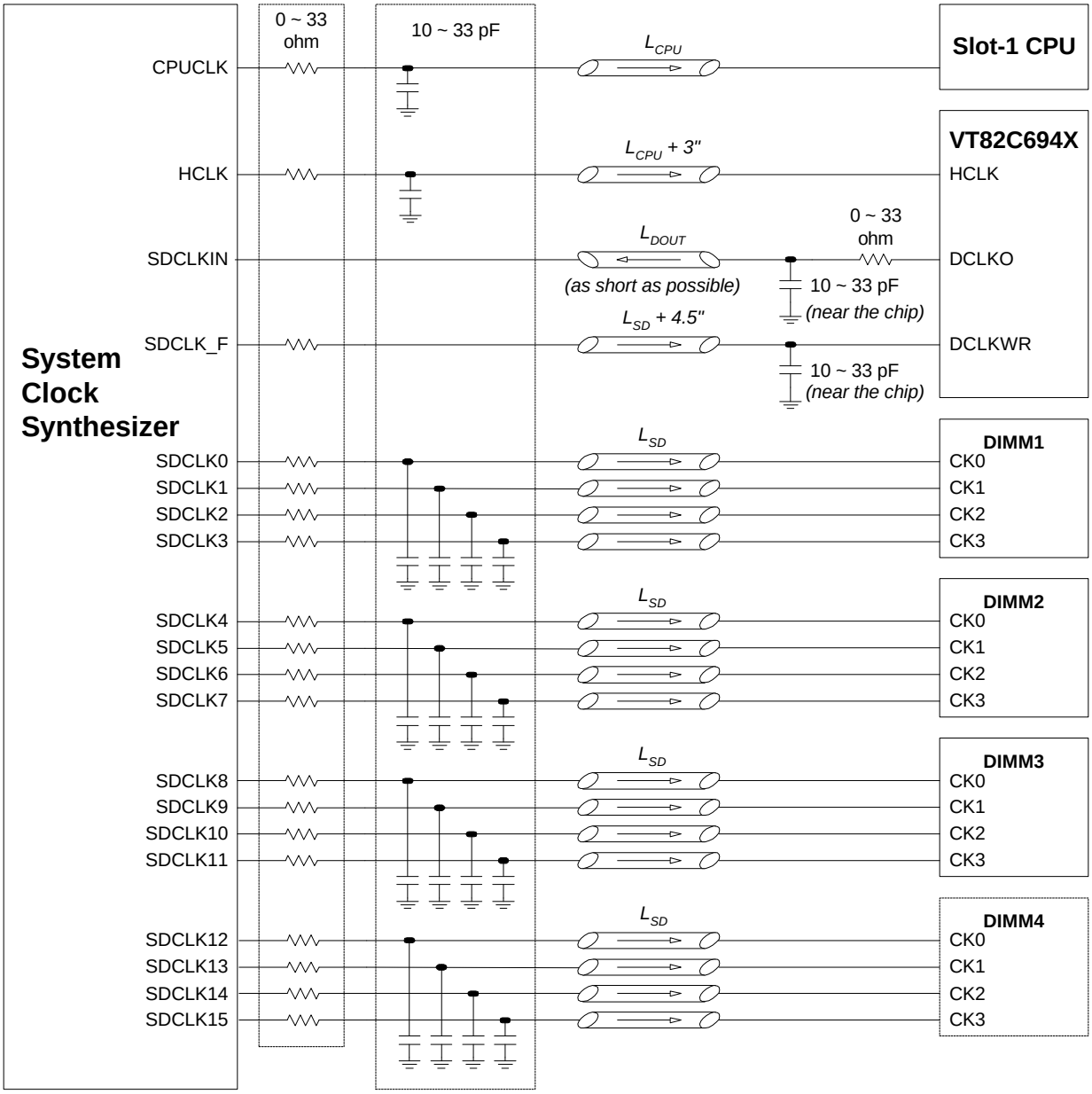


Figure 2-26. Host Clock and SDRAM Clock Layout Recommendations for Slot-1 System

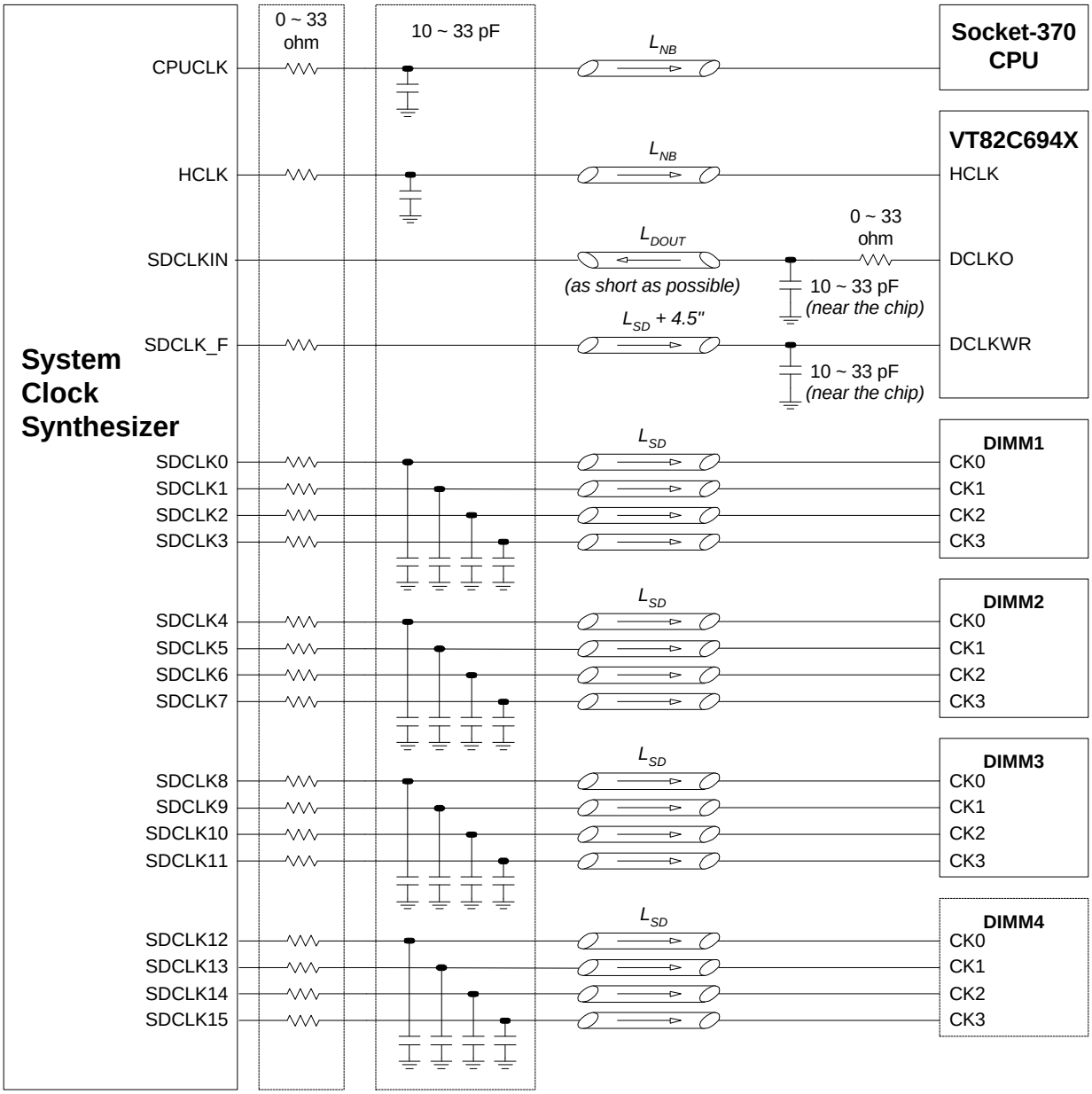


Figure 2-27. Host Clock and SDRAM Clock Layout Recommendations for Socket-370 Systems

2.3.2.6 AGP Clock Signals

Layout recommendations for the AGP clock are shown in Figure 2-28. Typically, 22 ohm series terminations are recommended for the AGP clock. A typical 22 pF bypass capacitor is also required for the AGP clock (GCLKO) to the AGP slot. Depending on how the system is designed, the value of the bypass capacitors for the PCI clocks may vary. For clock alignment considerations, 3 more inches than that of the AGP clock trace to the AGP slot are added to the feedback AGP clock trace length. (Note: the 3 inches represents the estimated distance from the GCLK pin of a AGP slot to the GCLK pin of the VGA chip on an AGP video card.) Some layout guidelines for the AGP clock are listed below:

- The trace length of the two separate GCLKO signals from pin N4 of the VT82C694X chip to the damping resistors should be equal and less than 1 inch.
- Both C1 and C2, which should be placed very close to the VT82C694X chip and the AGP slot respectively, are used to control the AGP clock alignment. (See Figure 2-28).

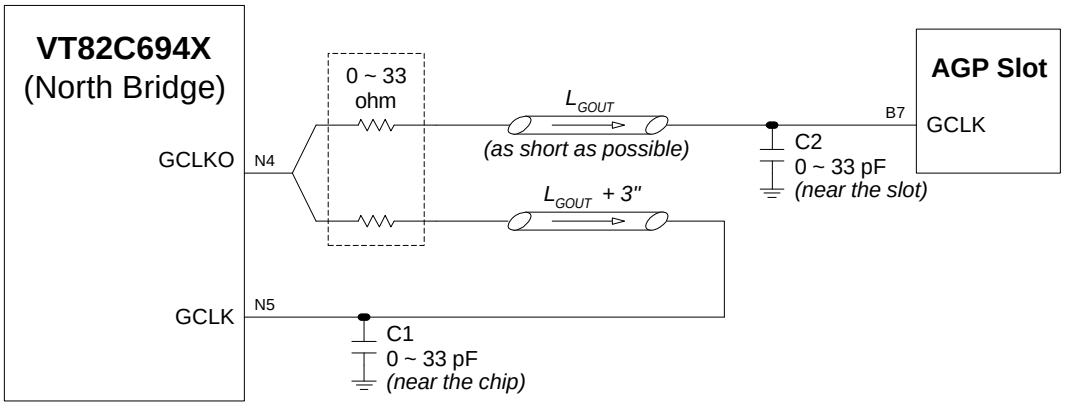


Figure 2-28. AGP Clock Layout Recommendations

2.3.2.7 PCI Clock Signals

Layout recommendations for the PCI clocks are shown in Figure 2-29. Typically, 22 ohm series terminations are recommended for all PCI clocks. A typical 22 pF bypass capacitor is also required for each PCI clock. Depending on how the system is designed, the value of the bypass capacitors for the PCI clocks may vary. For clock alignment considerations, trace lengths of all PCI clocks should match the longest one.

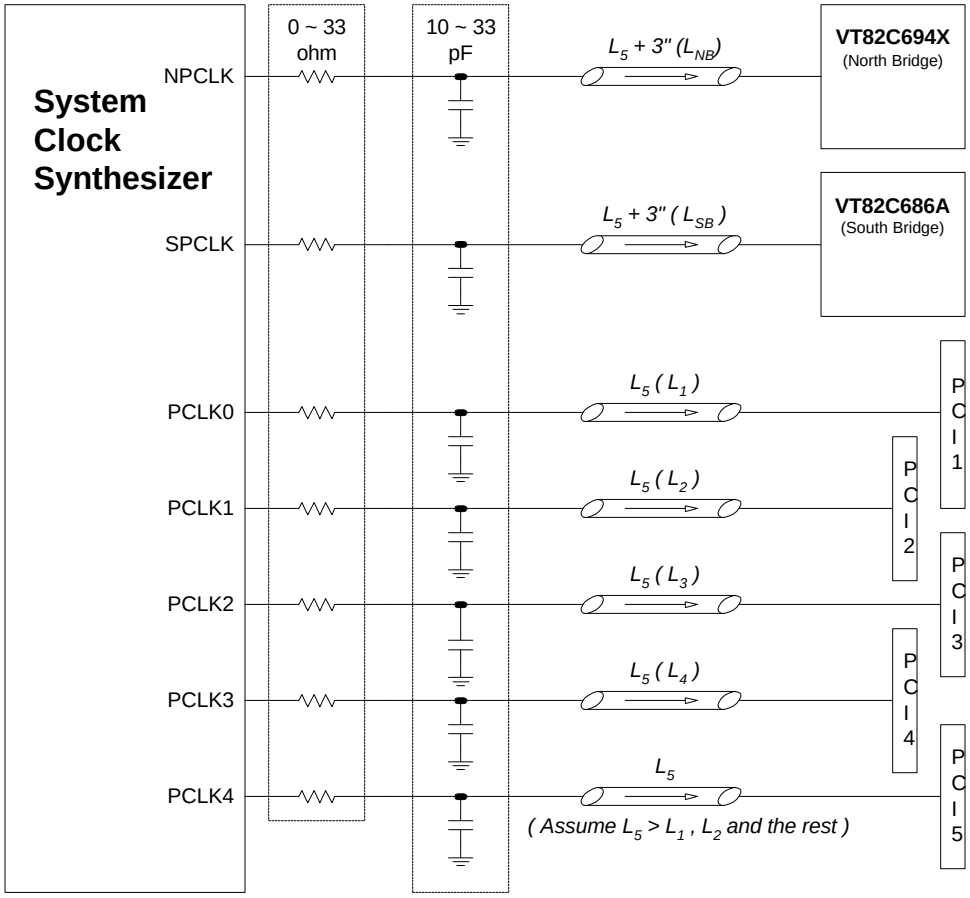


Figure 2-29. PCI Clock Layout Recommendations

2.3.2.8 Miscellaneous Clock Signals

22 ohm series terminations are recommended for clock signals such as the USB clock (48 MHz), Super I/O clock (typically 24 MHz), IOAPIC clock (14.31818MHz, 2.5V interface) and reference clock (14.31818 MHz, 3.3V interface) which are generated from the system clock synthesizer. The trace width for the clocks above should be at least 15 mils. To reduce crosstalk impact, trace spacing between these clocks and other signals should be maintained at a minimum of 15 mils. **In order to maintain the clock signal quality, the trace length of these clock signals, especially USBCLK, should be as short as possible or less than 9 inches.**

2.3.2.9 Clock Trace Length Calculation

The calculation is based on the recommended placements shown in sections 2.2.1 and 2.2.2. A different component placement may result in a different calculation for the clock trace length.

CPU Clock Trace Length Calculation for Slot-1 System

Before routing any other signals on the board, pre-route every CPU clock trace from the system clock synthesizer to the Slot-1 CPU (CPUCLK) and North Bridge (HCLK) as short as possible. All high frequency clock alignment will be on the basis of the longest one (usually CPUCLK around 3700 mils). Please refer to the component placements in figures 2-3 and 2-4. A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → CPU	L_{CPU}	**L_{CPU}**	-	1"~9"
Clock chip → VT82C694X (NB)	L_{NB}	**L_{CPU} + 3"**	0.5"	4"~12"

Note: Here, the 3" represents the estimated trace length added into HCLK for CPU clock alignment.

CPU Clock Trace Length Calculation for Socket-370 System

Before routing any other signals on the board, pre-route every CPU clock trace from the system clock synthesizer to the Socket-370 CPU (CPUCLK) and North Bridge (HCLK) as short as possible. All high frequency clock alignment will be on the basis of the longest one (usually HCLK around 5500 mils). Please refer to the component placements in figures 2-5 and 2-6. A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → CPU	L_{CPU}	**L_{NB}**	0.5"	1"~9"
Clock chip → VT82C694X (NB)	L_{NB}	**L_{NB}**	-	1"~9"

SDRAM Clock Trace Length Calculation

Pre-route SDRAM clock traces (SDCLK0~SDCLK11) from the system clock synthesizer to the DIMM slots as short as possible. The length of all SDRAM clocks will be based on the longest one (L_{SD}). The length of DCLKWR (L_{DIN}) should be the same as that of the SDCLKs. The DCLKO clock trace should be as short as possible. A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → SDCLK[15:0]	L_{SD}	**L_{SD}**	0.5"	1"~4"
DCLKWR (Clock chip → NB)	L_{DIN} (assume < L_{SD} +3")	**L_{SD} + 4.5"**	0.5"	4"~7"
DCLKO (NB → Clock chip)	L_{DOUT}	**L_{DOUT}**	-	1"~9"

Note: Here, the 4.5" represents the estimated trace length added into DCLKI for SDRAM clock alignment.

AGP Clock Trace Length Calculation

Pre-route AGP clock traces from the pin GCLKO of the VT82C694X to the AGP slot as short as possible. Then the trace length for the signal GCLK should be the GCLKO trace length plus 3 inches.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
GCLKOUT (NB → AGP Slot)	L_{GOUT}	**L_{GOUT}**	-	1"~9"
GCLKIN (NB → NB)	L_{GIN}	**L_{GOUT} + 3"**	0.5"	4"~12"

Note: Here, the 3" represents the estimated trace length added into GCLKI for AGP clock alignment.

PCI Clock Trace Length Calculation

Pre-route PCI clock traces from the system clock synthesizer to the VT82C694X (NPCLK) and VT82C686A (SPCLK) as short as possible. Then pre-route PCI clock traces PCLK0~PCLK4 from the system clock synthesizer to all PCI slots as short as possible. The length of these clocks will be based on the longest one (L_5). Usually PCI5 is the farthest PCI slot from the North Bridge chip. A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → VT82C694X (NB)	L_{NB}	**L_5 + 3"**	1"	4"~15"
Clock chip → VT82C686A (SB)	L_{SB}	**L_5 + 3"**	1"	4"~15"
Clock chip → PCI1	L_1	**L_5**	1"	1"~12"
Clock chip → PCI2	L_2	**L_5**	1"	1"~12"
Clock chip → PCI3	L_3	**L_5**	1"	1"~12"
Clock chip → PCI4	L_4	**L_5**	1"	1"~12"
Clock chip → PCI5	L_5 (> the others)	**L_5**	-	1"~12"

Note: Here, the 3" represents the estimated trace length added into NPCLKI and SPCLK for PCI clock alignment.

Notes for the length calculation of all clock traces:

1. *Shortest length means the minimum routable trace length between both clock ends.*
2. *Desired length means the real length of the clock traces on PCB layout.*
3. *Allowable difference means the maximum length difference between clock traces of the same type.*
4. *Allowable range means the acceptable clock length range for the specific clock.*
5. *The location of the system clock chip can affect the length of all clock traces. To optimize the clock alignment, place the clock chip at an appropriate location.*
6. *In addition, the trace impedance of all clock traces should be in the range of 40 ohms and 55 ohms.*

2.3.3 Routing Styles and Topology

High-speed bus signals are sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. In order to maintain better signal quality, transmission stubs should be kept under 1.5 inches. Therefore, daisy chain style routing is strongly recommended for these signals. Figure 2-30 below shows an example of a daisy chain routing.

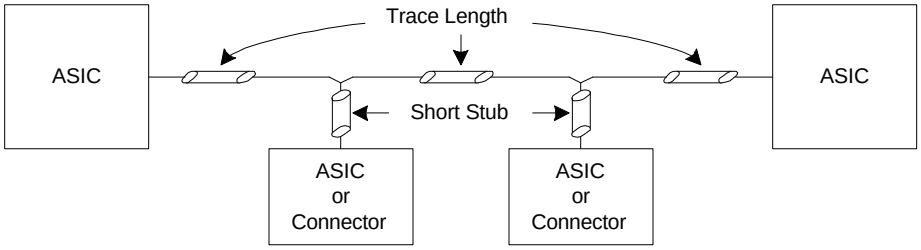


Figure 2-30. Daisy Chain Routing Example

Topology is the physical connectivity of a net or a group of nets. Basically, there are two types of topologies for a motherboard layout: point-to-point and multi-drop. An example of these topologies is shown in Figure 2-31.

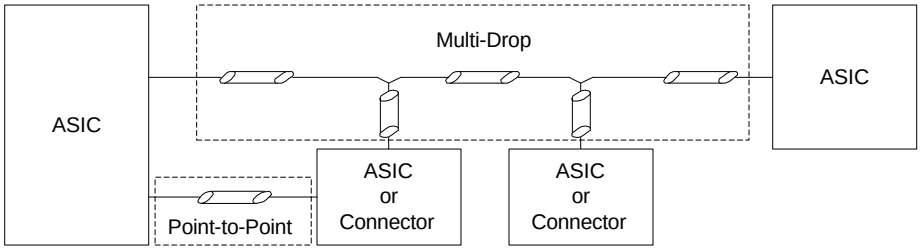


Figure 2-31. Point-to-Point and Multi-Drop Topology Examples

If daisy chain routing is not allowed in some circumstances, different routings may be considered. An alternative topology is shown in Figure 2-32. The branch point in this case is somewhere between both ends. It may be near the source or near the loads. Being close to the load side is best. The separated traces should be equal length.

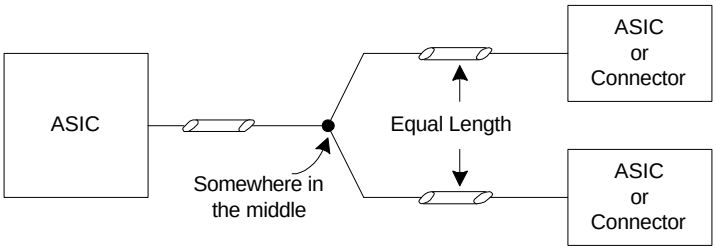


Figure 2-32. Alternate Multi-Drop Topology Example

2.4 VT82C694X Apollo Pro133A Layout and Routing Guidelines

2.4.1 Host CPU Interface Layout and Routing Guidelines

The GTL+ signals (host address bus, host data bus and host control signals) are typical point-to-point connections between CPU and North Bridge in a Slot-1 or Socket-370 system design. VTT (1.5V) terminations are required for GTL+ signals. Except for FERR#, all host control signals from the VT82C686A South Bridge to Slot-1 or Socket-370 CPU are open drain (OD) signals. 2.5V pull-ups are required for those open drain signals on the VT82C686A chip side. The routing topology for both signal groups from VT82C694X and VT82C686A uses point-to-point connections. Recommended layout guidelines and routing examples for GTL+ and OD signals are given in the following sections.

2.4.1.1 Slot-1 Host Interface to North Bridge

The recommended topology for Slot-1 host signals to the North Bridge (VT82C694X) is shown in Figure 2-33. For signal quality considerations, the trace length of the host address bus should be minimized. No VTT terminations are required for a Slot-1 system since they are built in to both the Slot-1 CPU and the VT82C694X.

- It is recommended to route all host signals to the VT82C694X in equal length and as short as possible. A minimum of 5 mils in width and a minimum of 10 mils in spacing are required for those host signals. The trace length of those signals should be less than 4.5 inches.

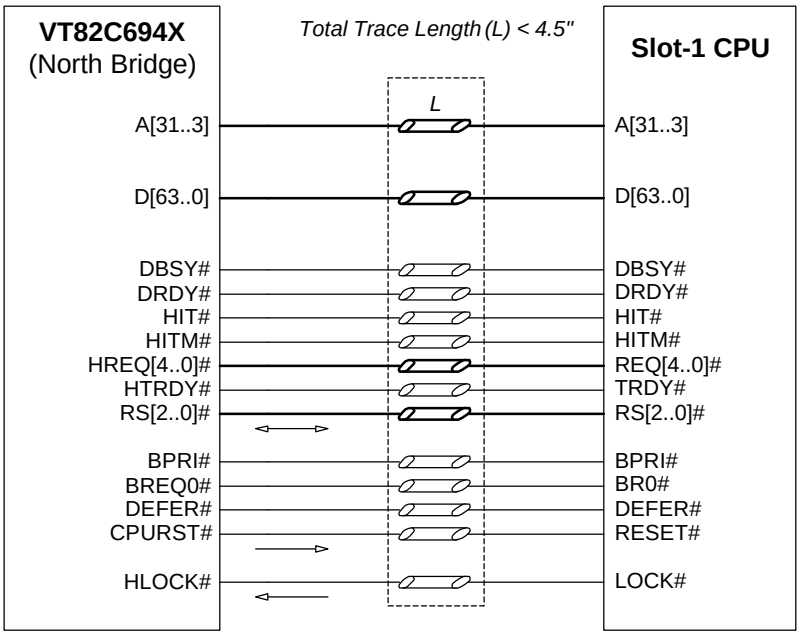


Figure 2-33. Slot-1 Host Interface Topology Example

2.4.1.2 Socket-370 Host Interface to North Bridge

The recommended topology for the Socket-370 host signals to North Bridge (VT82C694X) is shown in Figure 2-34. For signal quality considerations, the trace length of the host signals should be minimized. 56 ohm pull-ups to VTT near the Socket-370 CPU are required.

- It is recommended to route all host signals to VT82C694X in equal length and as short as possible. A minimum of 5 mils in width and a minimum of 10 mils in spacing are required for those host signals. Wide traces for VTT pull-ups are recommended.
- There is no stub before traces L1 and L2. Two traces directly come out the pin of the Socket-370. The location of these 56 ohm resistor networks should be as close to Socket-370 CPU as possible.
- The most qualified range of the L1 trace length is between 1.5 inches and 4.5 inches. The trace length of L2 should be less than 2 inches.

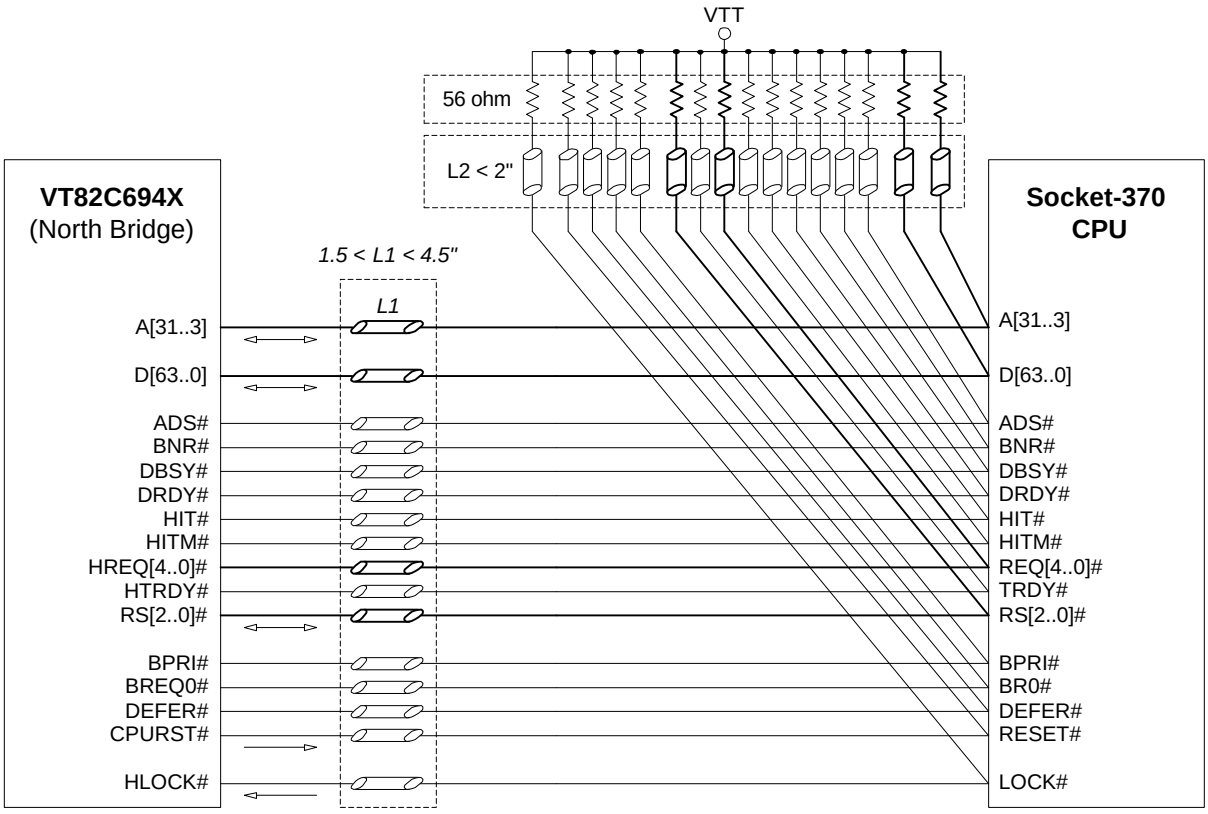
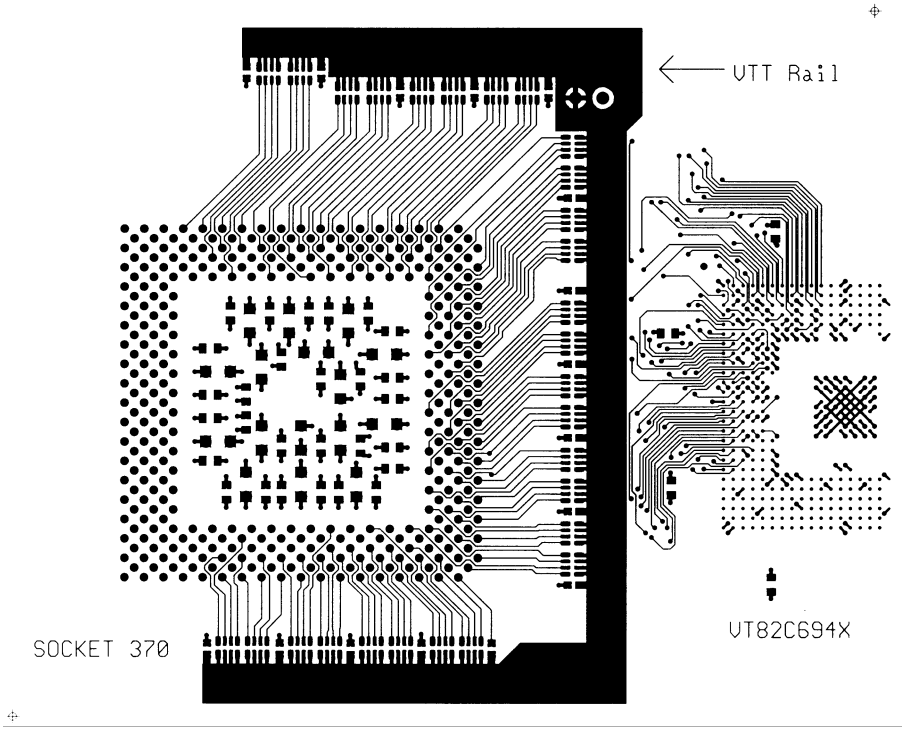
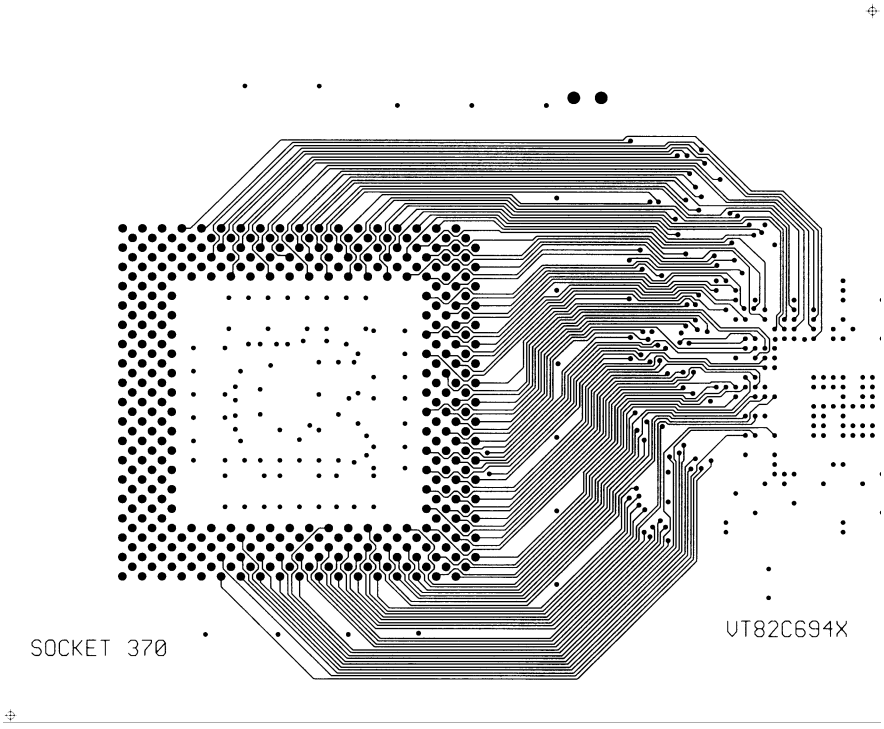


Figure 2-34. Socket-370 Host Interface Topology Example

A layout example for the host interface between the Socket-370 CPU and the VT82C694X chip is shown in Figure 2-35. The VTT rail (a minimum of 200 mils wide) covering three sides of the Socket-370 on the component layer can provide a sufficient GTL+ termination voltage supply path in Figure 2-35 (a).



(a) Component Side



(b) Solder Side

Figure 2-35. Host Interface Layout Example between Socket-370 and VT82C694X

2.4.1.3 CPU Host Interface to South Bridge

The host control signals from the Slot-1 or Socket-370 CPU to the south bridge (VT82C686A) are listed in Table 2-9. Except for FERR#, all signals are open drain (OD). 2.5V pull-ups are required for those open drain signals on the VT82C686A chip side.

Table 2-9. Host Control Signals to South Bridge

South Bridge -- CPU		
Signal Name	**I/O**	**Description**
A20M#	OD	A20 Mask
CPURST	OD	CPU Reset
FERR#	I	Numerical Coprocessor Error
IGNNE#	OD	Ignore Numerical Error
INIT	OD	Initialization
INTR	OD	CPU Interrupt
NMI	OD	Non-Maskable Interrupt
SLP#	OD	Sleep
STPCLK#	OD	Stop Clock
SMI#	OD	System Management Interrupt

In a Slot-1 system design, pins A20M#, IGNNE#, INTR (LINT0) and NMI (LINT1) are shared with the external CPU clock ratio straps. The schematic for this pin sharing is shown in Figure 2-36. These pins strap the setting of the CPU clock ratio during reset and two clocks beyond the end of the RESET# pulse. Afterwards, the functionality of these signals will work as their names are defined. (Note: This ratio select logic is also required in the Q-Spec Socket-370 system design.)

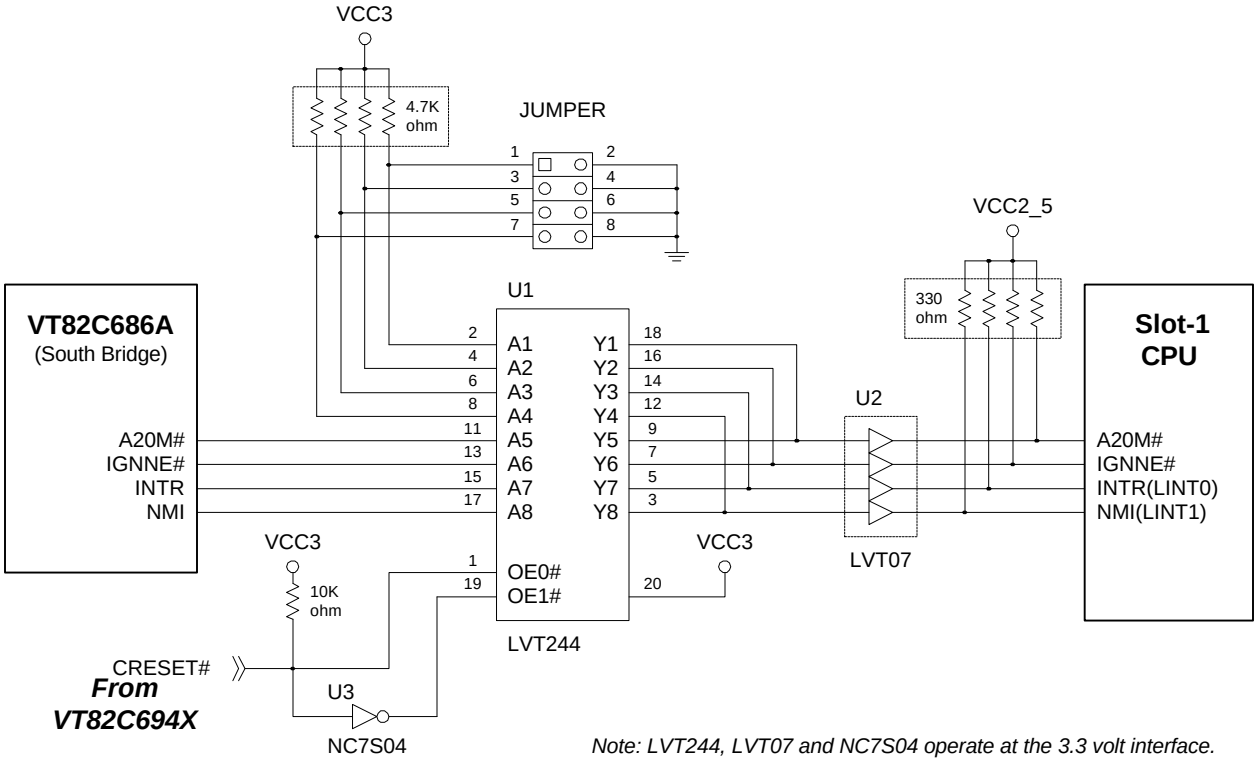


Figure 2-36. Schematic Example for Slot-1 CPU Internal/External Clock Ratio Pin Sharing

A layout example for the remaining control signals between the VT82C686A chip and the Slot-1 CPU is shown in Figure 2-37.

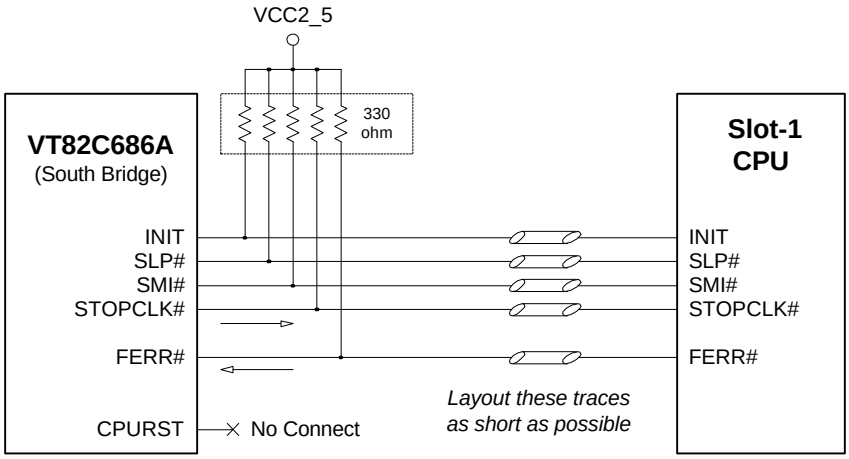


Figure 2-37. Layout Example of Control Signal from South Bridge to Slot-1 CPU

No sharing circuitry is required in an S-Spec Socket-370 system design because the S-Spec Socket-370 CPU runs at marked ratio only. A layout example for all control signals between the VT82C686A chip and the Socket-370 CPU is shown in Figure 2-38. Currently, the voltage level of VCC_CMOS is 2.5V.

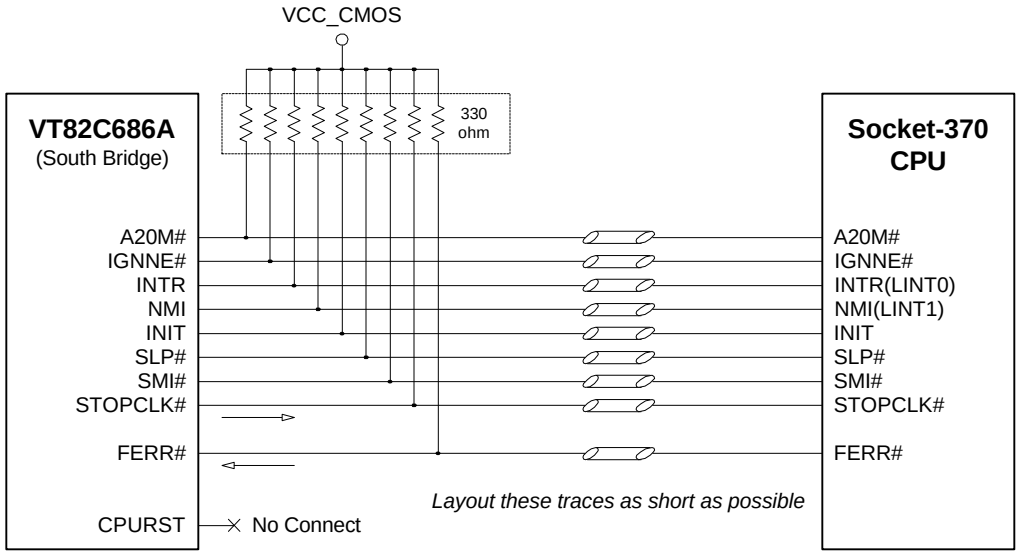


Figure 2-38. Layout Example of Control Signal from South Bridge to Socket-370 CPU

The layout guidelines for these signals from the Slot-1 or Socket-370 CPU to the south bridge (VT82C686A) are listed below.

- Each south bridge Open Drain (OD) output control signal to the CPU needs a 150 ~ 450 ohm pull-up which should be placed as close to the VT82C686A chip as possible.
- A minimum of 5 mils in width and a minimum of 10 mils in spacing are sufficient for good signal quality.
- No specific limitation of the trace length for these control signals is required.

2.4.2 Memory Subsystem Layout and Routing Guidelines

2.4.2.1 DRAM Routing Guidelines

Most DRAM signals are multi-drop connections. A brief description of the memory subsystem signals is provided in Table 2-10 below.

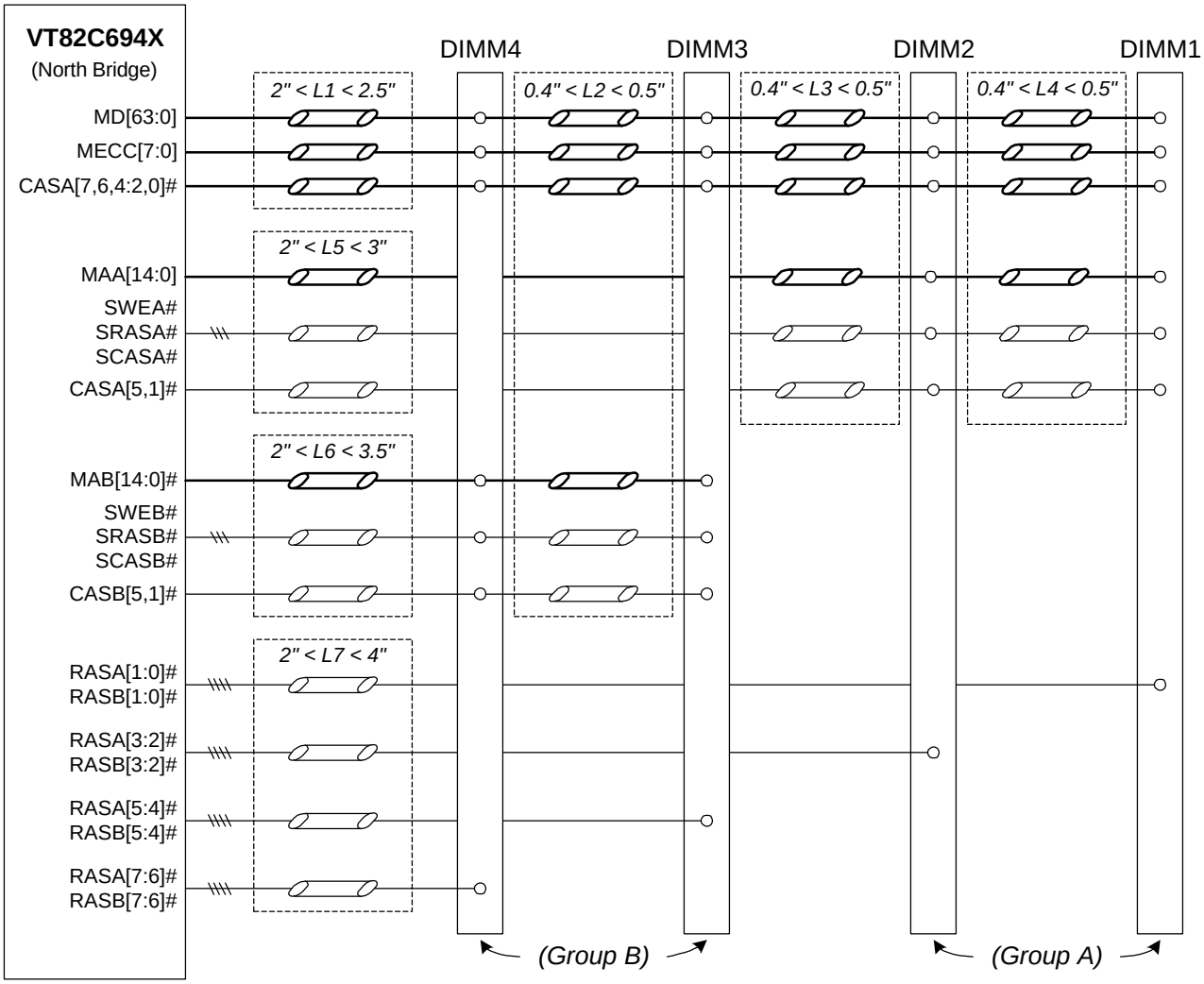
Table 2-10. Memory Subsystem Signals

North Bridge -- DRAM		
Signal Name	**I/O**	**Description**
MAA[14:0]	O	Memory Address for the group A
MAB[14:11]#, MAB10, MAB[9:0]#	O	Memory Address for the group B
MD[63:0]	IO	Memory Data for all four DIMM modules
MECC[7:0]	IO	DRAM ECC or EC Data for all four DIMM modules
RASA[5:0]#	O	Row Address Strobe of each bank
RASB[5:0]#	O	Row Address Strobe of each bank
CASA[7:0]#	O	Column Address Strobe of each byte lane for the group A
CASB5#, CASB1#	O	Column Address Strobe of each byte lane for the group B
SRASA#	O	Row Address Command Indicator for the group A
SRASB#	O	Row Address Command Indicator for the group B
SCASA#	O	Column Address Command Indicator for the group A
SCASB#	O	Column Address Command Indicator for the group B
SWEA#	O	Write Enable Command Indicator for the group A
SWEB#	O	Write Enable Command Indicator for the group B

Note: Group A represents the first two DIMM modules and group B represents the remaining (one or two) modules. CASA[7:6, 4:2, 0]# can also be connected to the DIMM modules of group B.

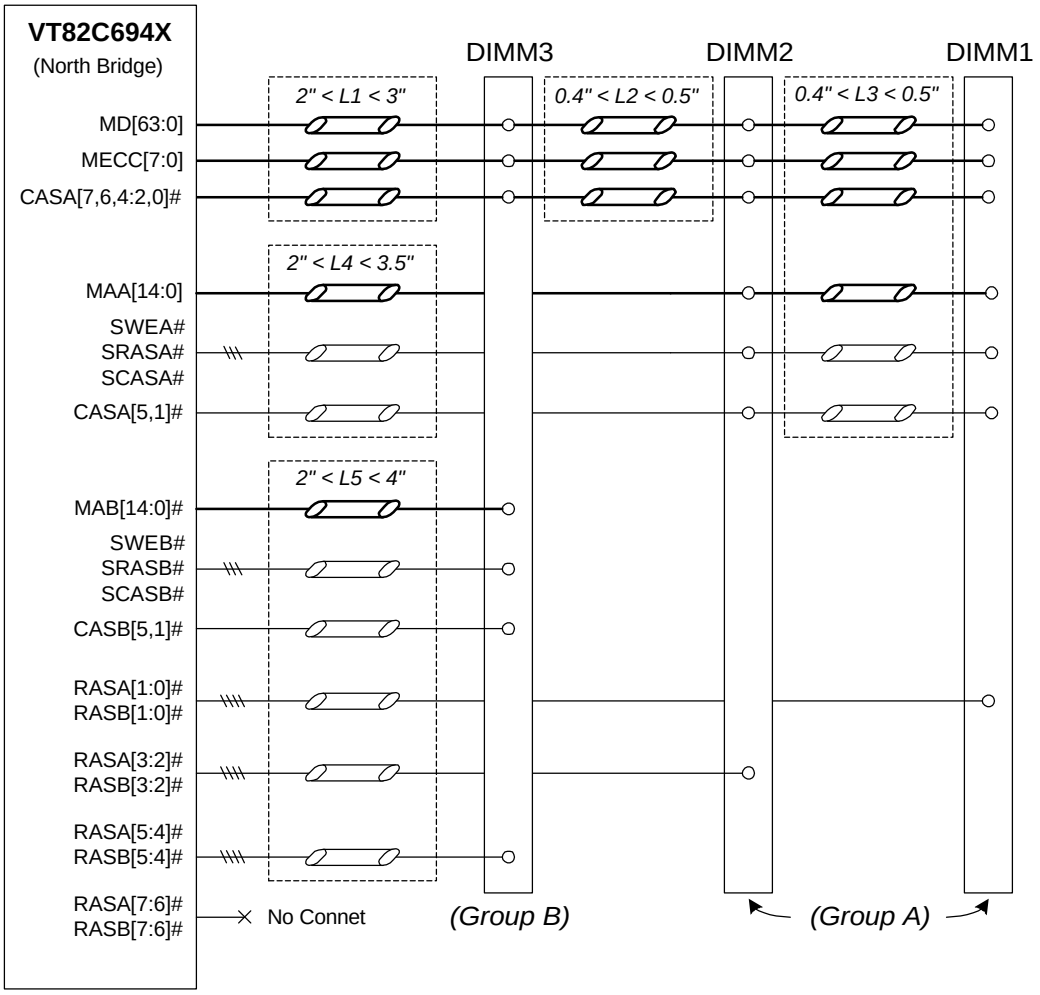
The maximum DRAM installation is four DIMM slots. Three layout examples (Daisy Chain Ordering) for all DRAM buses and control signals between the Apollo Pro133A North Bridge and four, three or two DRAM DIMM slots are shown in Figure 2-39, 2-40 and 2-42 respectively. One T-Style layout example for DRAM signals, such as MD[63:0] and MECC[7:0], between the Apollo Pro133A North Bridge and three DRAM DIMM slots is shown in Figure 2-41. Routing recommendations for the DRAM interface are listed below.

- Traces for all DRAM signals should be a minimum of 5 mils in width and 10 mils in spacing. The accumulated trace length for all signals should be under 4 inches to meet 133 MHz timing requirements. The length difference among traces should be minimized.
- The DRAM interface damping resistors are no longer needed.
- For daisy chain routing, traces of MD[63:0], CASA[7:0]# and MECC[7:0] should be connected to the DIMM modules in order of DIMM4, DIMM3, DIMM2 and DIMM1 (see Figure 2-39). DIMM4 is the closest DIMM slot to the VT82C694X chip.
- It is recommended to make segments L2, L3 and L4 as short as possible in Figure 2-39.



Note: MAB[14:0]# represents MAB[14:11]#, MAB10 and MAB[9:0]#.

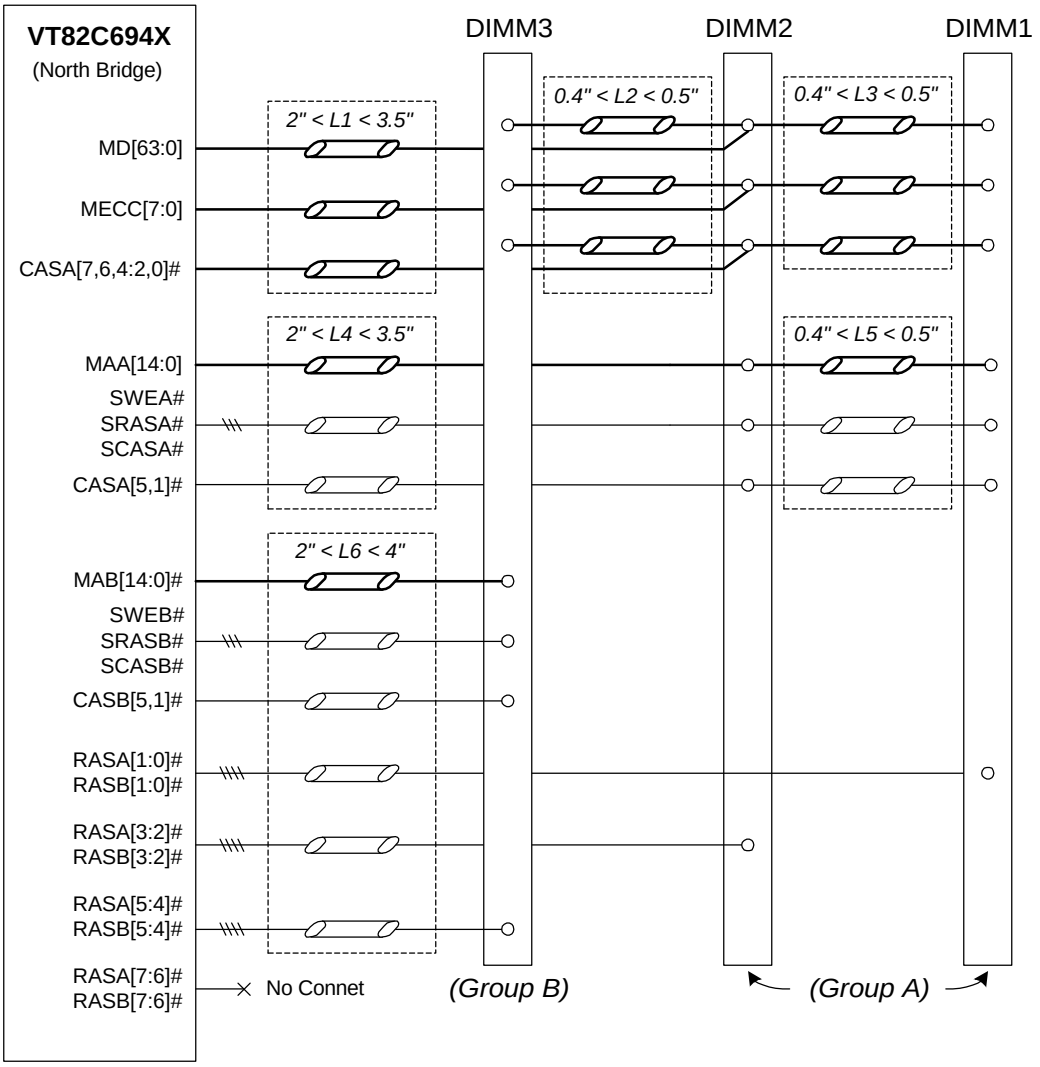
Figure 2-39. Daisy Chain Routing for Four-DRAM DIMM Slots



Note: MAB[14:0]# represents MAB[14:11]#, MAB10 and MAB[9:0]#.

Figure 2-40. Daisy Chain Routing for Three-DRAM DIMM Slots

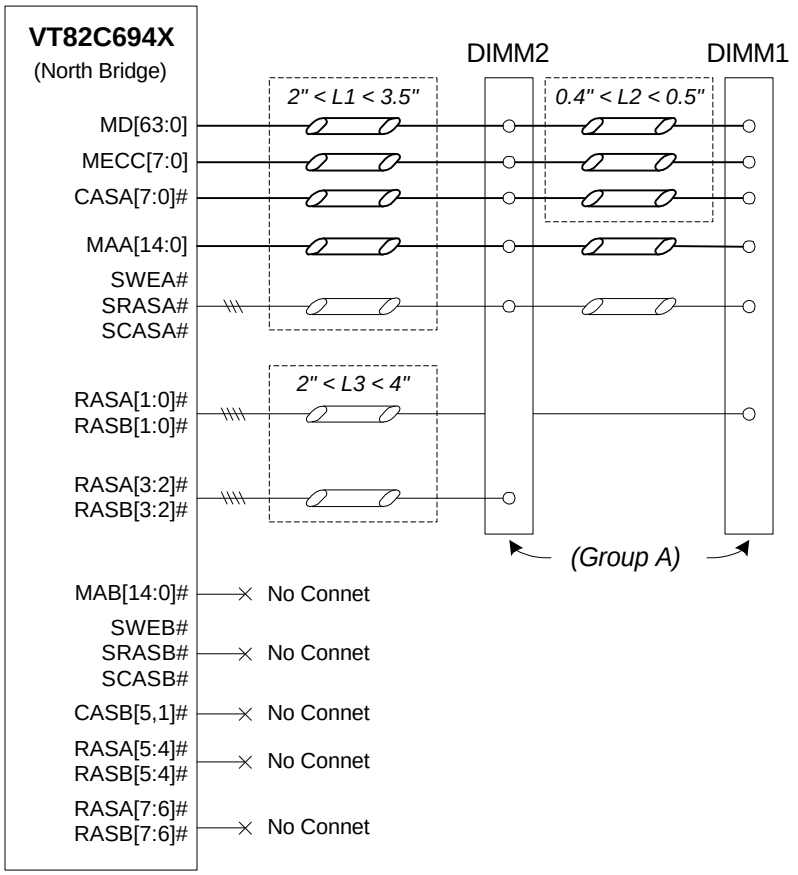
Note: Comparing to T-Style routings in Figure 2-41, the advantages of Daisy Chain Ordering routings are lower crosstalk between traces, easier layout.



Note: MAB[14:0]# represents MAB[14:11]#, MAB10 and MAB[9:0]#.

Figure 2-41. T-Style Routing for Three-DRAM DIMM Slots

Note: Comparing to Daisy Chain Ordering routings in Figure 2-40, the advantage of T-Style routings is less signal reflection on traces.



Note: MAB[14:0]# represents MAB[14:11]#, MAB10 and MAB[9:0]#.

Figure 2-42. Daisy Chain Routing for Two-DRAM DIMM Slots

2.4.2.2 DRAM Reference Layout

Maintaining DRAM trace length less than 4 inches is required to fulfill 133 MHz DRAM timing requirements. A placement example of the VT82C694X chip and 3 DIMM slots is shown in Figure 2-43. The VT82C694X chip is located at the top of the middle of 3 DIMM slots. The distance between the chip and the closest DIMM slot (DIMM3) is 0.55 inch. The distance between the centers of two adjacent DIMM slots is 0.4 inch.

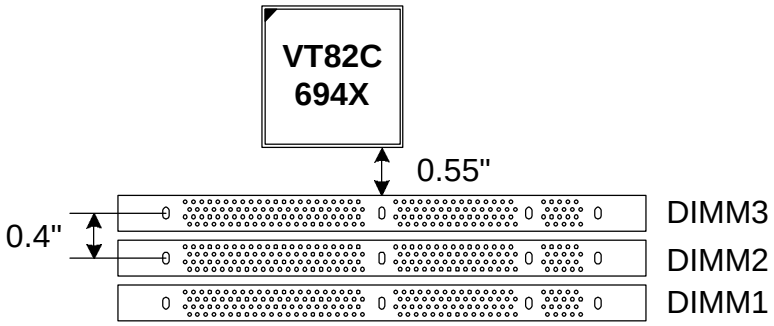
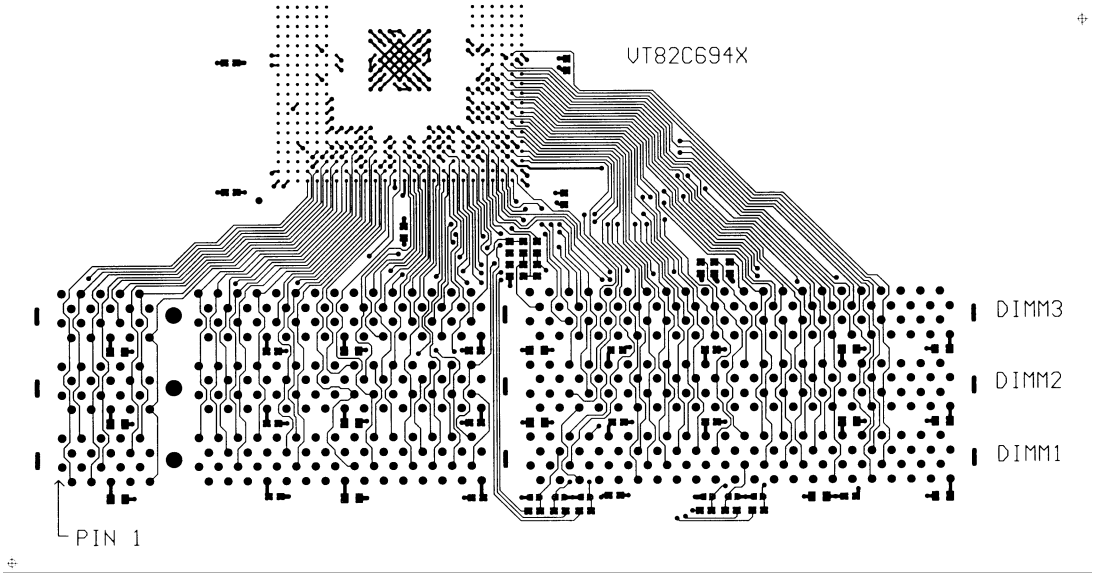
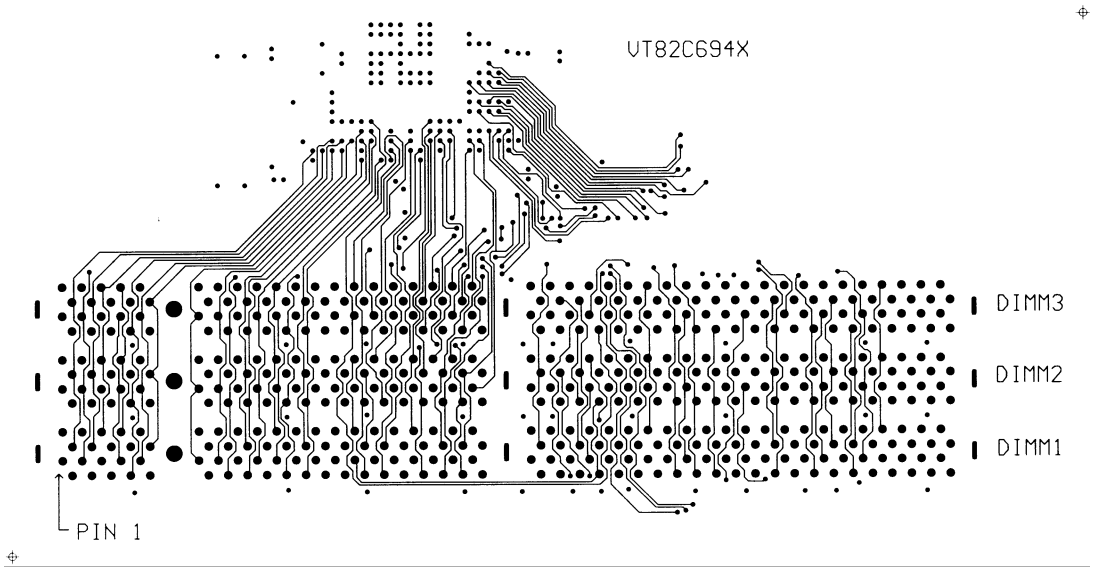


Figure 2-43. DRAM Placement for 133MHz Timing Consideration

The reference layout for three-DRAM DIMM slots is shown in Figure 2-44 below. In this layout example, no DRAM trace is over 4 inches long and those traces are also evenly distributed.



(a) Component Side



(b) Solder Side

Figure 2-44. Layout Example of Three-DRAM DIMM Slots

2.4.3 AGP (4X Mode) Interface Layout and Routing Guidelines

This section describes layout and routing guidelines to insure a robust AGP 4X mode interface design. The following guidelines will help insure that the AGP specification can be met. The system designer should do appropriate analysis and simulation to verify that the design fulfills AGP specification requirements.

2.4.3.1 General Layout and Routing Recommendations

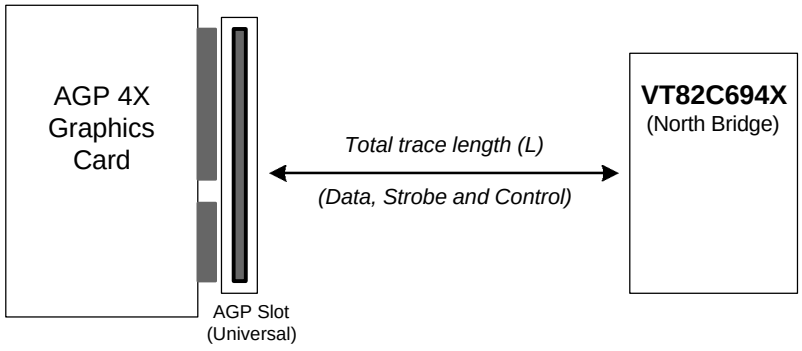
There are three major groups of AGP control, data and their associated strobe signals listed in Table 2-11. The remaining AGP signals include AGPVREF (AGP reference voltage input), GCLK and GCLKO (AGP clock input and output), VDDQ/GND (power/ground) and NCOMP and PCOMP (digital compensation).

Table 2-11. VT82C694X AGP 4X Signal Groups

AGP Signal Groups	VT82C694X (4X mode)
Data / Strobe	Group 1: GD[15:0], GBE[1:0]# / GDS0 and GDS0#
	Group 2: GD[31:16], GBE[3:2]# / GDS1 and GDS1#
	Group 3: SBA[7:0] / SBS and SBS#
Control	GFRM#, GIRDY#, GTRDY#, GSTOP#, GDSEL#, GPIPE#, GRBF#, ST[2:0], GREQ#, GGNT#, GPAR and GWBF# (14 signals)

Note: The AGP signal naming convention here (and in the VT82C694X datasheet) is slightly different from that in the AGP Specification.

General routing guidelines for the connections between the VT82C694X chip and the AGP slot are shown in Figure 2-45. These guidelines were created to give freedom to designs by making tradeoffs between signal coupling and line length. However, AGP signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification.

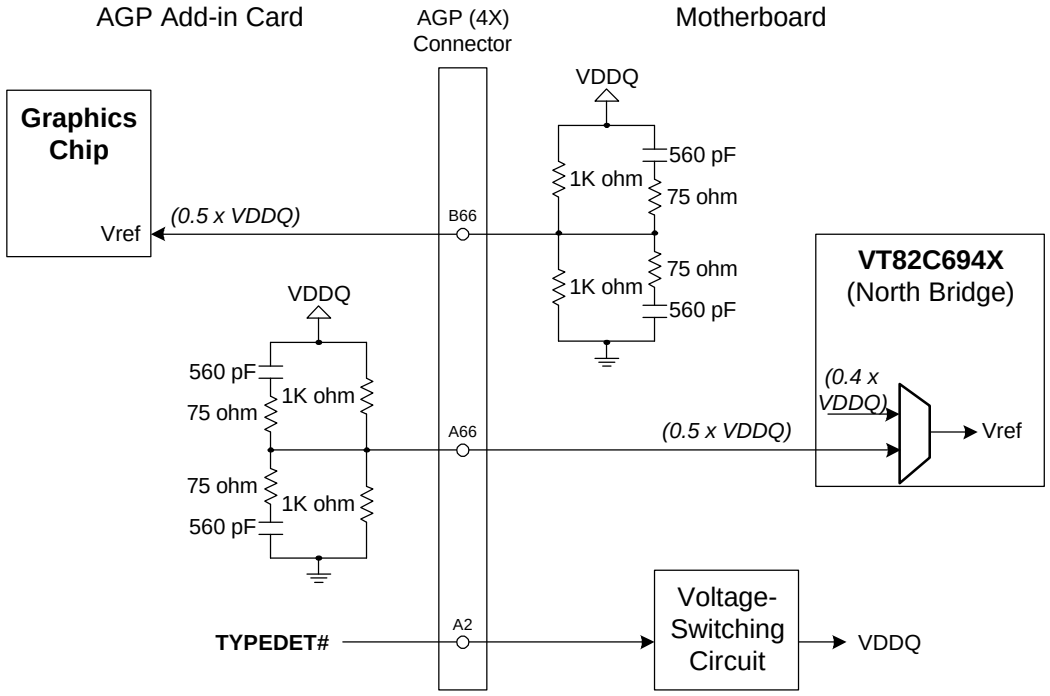


Guidelines:
1. Data and Control (width:Spacing) Routings are (1:3) in the range of 1" < L < 4".
2. Strobe Routings are (1:4) to Strobe and (1:6) to other signals.
3. The recommended motherboard impedance for AGP 4X is 65 ohm +/- 5 ohm.

Figure 2-45. General Layout Recommendations of AGP 4X Interface

2.4.3.2 Vref Characteristics for AGP 4X Mode

Vref is a DC voltage reference signal used to set the input sense level on the AGP bus. Vref is set at 0.5 x VDDQ (between 0.48 x VDDQ and 0.52 x VDDQ) for AGP 4X mode. Referring to Figure 2-46 for an AGP 4X mode implementation, two unidirectional Vref pins are provided in the connector. These pins connect Vref between the add-in card graphics chip and the VT82C694X chip. Typical values of the resistors and capacitors in the voltage divider network are shown in the figure. The Vref resistor divider network must be placed away from critical and noisy signals, especially 3.3V swing signals. Guard (ground) trace should be implemented if adjacent to 3.3V swing signal cannot be avoided. To avoid signal crosstalk from other signal lines, the trace to the Vref input pin should be kept away from other noisy traces in the board layout. Decoupling capacitors should not be implemented directly on Vref for better tracking between VDDQ and Vref.



Note: TYPEDET# provided by the AGP add-in card is used to determine the VDDQ (1.5V or 3.3V) through a switching or linear regulator.

Figure 2-46. AGP 2X and 4X Mode Sharing Circuit

2.4.3.3 AGP VDDQ Power Delivery

AGP 2X (or 1X) mode can operate in either 3.3V interface or 1.5V interface. However, AGP 4X mode uses only 1.5V interface. For sharing of both AGP interfaces, switching between two different voltage supplies (3.3V and 1.5V) for the AGP slot should be taken into account. Refer to Figure 2-46 above for the AGP 2X and 4X mode sharing circuit. Pin A2 (TYPEDET#) of the AGP slot is used to determine the AGP operating voltage (VDDQ) through the voltage switching circuit. For example, the AGP interface is 1.5V if the TYPEDET# is shorted to ground (or activated to low) on the add-in card side. However, when TYPEDET# is open (not connected to any power rail or signal), the voltage switching circuit outputs 3.3V VDDQ. At the same time, Vref of 0.4 x VDDQ for 3.3V signaling is internally generated in VT82C694X and external Vref of 0.5 x VDDQ for 1.5V signaling on board is disconnected.

In the case of a universal 1.5V / 3.3V signaling system, an on-board voltage regulator is preferred. The voltage level of the regulator is controlled by the TYPEDET# signal which is controlled by the add-in card.

Figure 2-47 shows an application example for the VDDQ Voltage-Switching circuit shown in Figure 2-46. Signal TYPEDET# is used to determine the VDDQ voltage level (1.5V or 3.3V) for the AGP interface. When TYPEDET# is high, Q1 is always turned on. The VDDQ output voltage is provided directly by the VCC3 (3.3V). When TYPEDET# is low, the VDDQ output voltage is 1.5V by regulating the VCC3 power source through the SC1105 switching regulator.

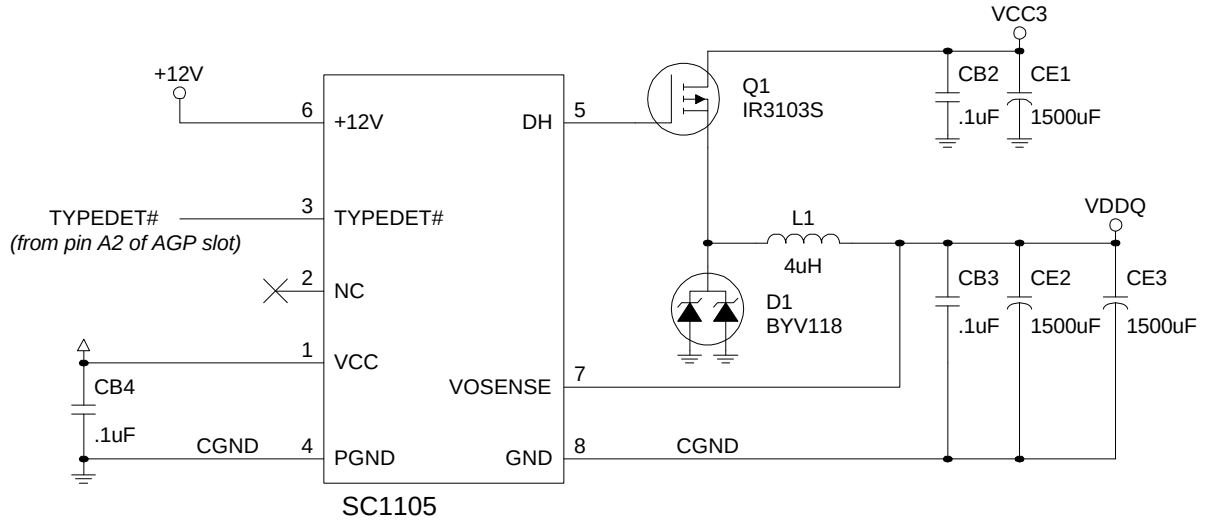


Figure 2-47. VDDQ Voltage-Switching Application Circuit

Figure 2-48 shows another application example for the VDDQ Voltage-Switching circuit. When TYPEDET# is low, Q1 is turned off and a fixed 1.5V output is generated by the CS5257A-1GDP5 linear regulator (U1) to VDDQ. When TYPEDET# is high, Q1 is always turned on. The VDDQ output voltage is provided directly by the VCC3 (3.3V). At the same time, U1 is shut down due to a higher output voltage (3.3V VDDQ > fixed 1.5V output).

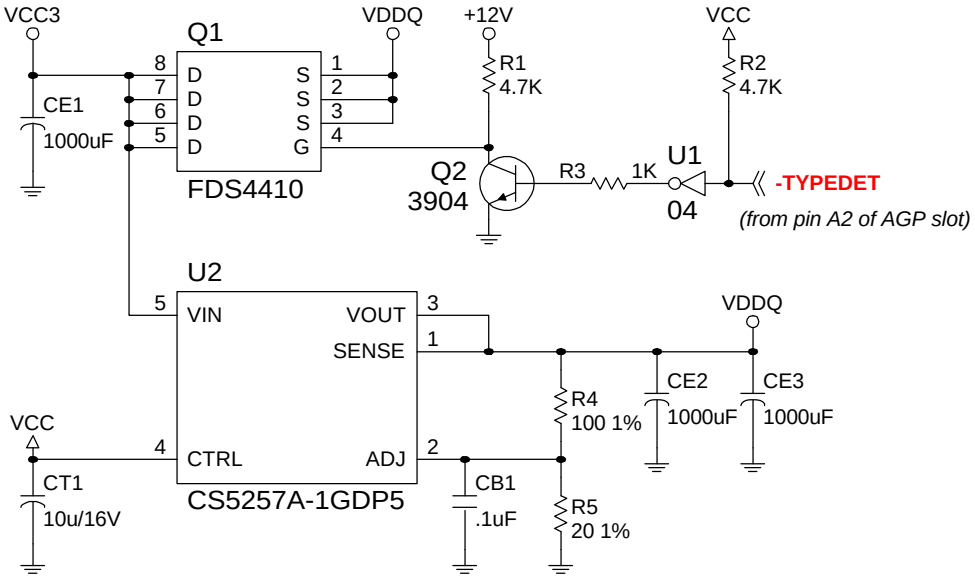


Figure 2-48. VDDQ Voltage-Switching Application Circuit (II)

2.4.3.4 AGP VDDQ Power Plane Partition

By referring to the power plane partition examples in figures 2-15 to 2-16, the power plane for the AGP slot should be separated from the remaining power planes on the motherboard. A VDDQ Island (selected area) will cover most of the AGP signal routing area. The detailed VDDQ power plane partition is shown in Figure 2-49.

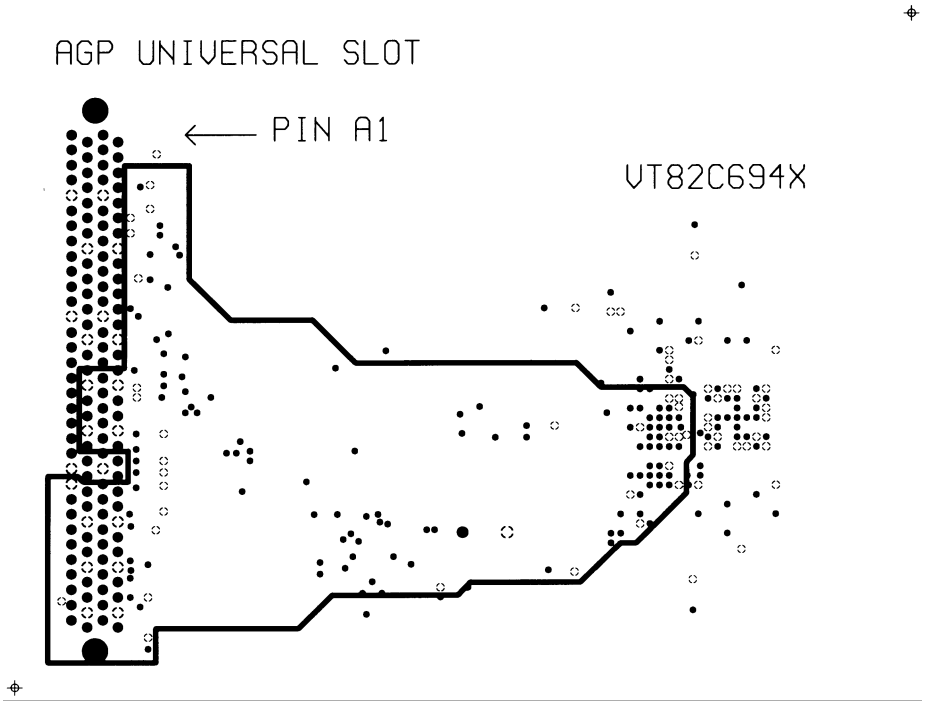


Figure 2-49. AGP VDDQ Power Plane Partition Example

2.4.3.5 Optimized Layout and Routing Recommendations

It is strongly recommended to maintain the trace length of all AGP (especially Data and Strobe) signals less than 4 inches. It is always best to reduce line mismatch to add to the timing margin. In other words, a balanced topology can match trace lengths within the groups to minimize skew. To minimize signal crosstalk, wider spacing is recommended wherever possible between traces. A layout example of the AGP interface between the VT82C694X and the AGP Slot is shown in Figure 2-50. Optimized layout and routing recommendations are listed below:

- Except strobe signals, traces for other AGP signals in Table 2-11 should be a minimum of 5 mils in width and 15 mils in spacing. The trace width of these six strobe signals should be 5 mils. The spacing for each strobe signal should be a minimum of 20 mils to other strobe signals and a minimum of 30 mils to non-strobe signals. Refer to Figure 2-51 for more detail on layout.

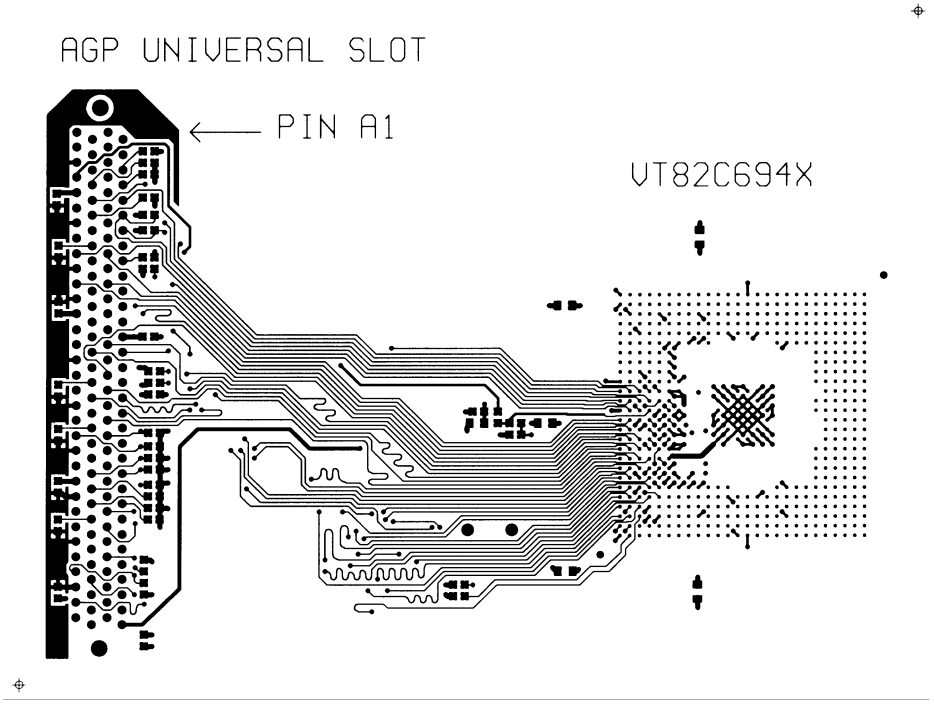
- The trace width of AGP clock signals (GCLKI and GCLKO) is at least 10 mils. The spacing for any AGP clock signal should follow the spacing requirements of its adjacent (Data, Strobe or Control) signal to limit signal coupling.

- The accumulated trace length for all signals in Table 2-11 should be less than 6 inches to limit signal coupling between traces. Trace length mismatch in any Data/Strobe group should be maintained within 0.5 inch.

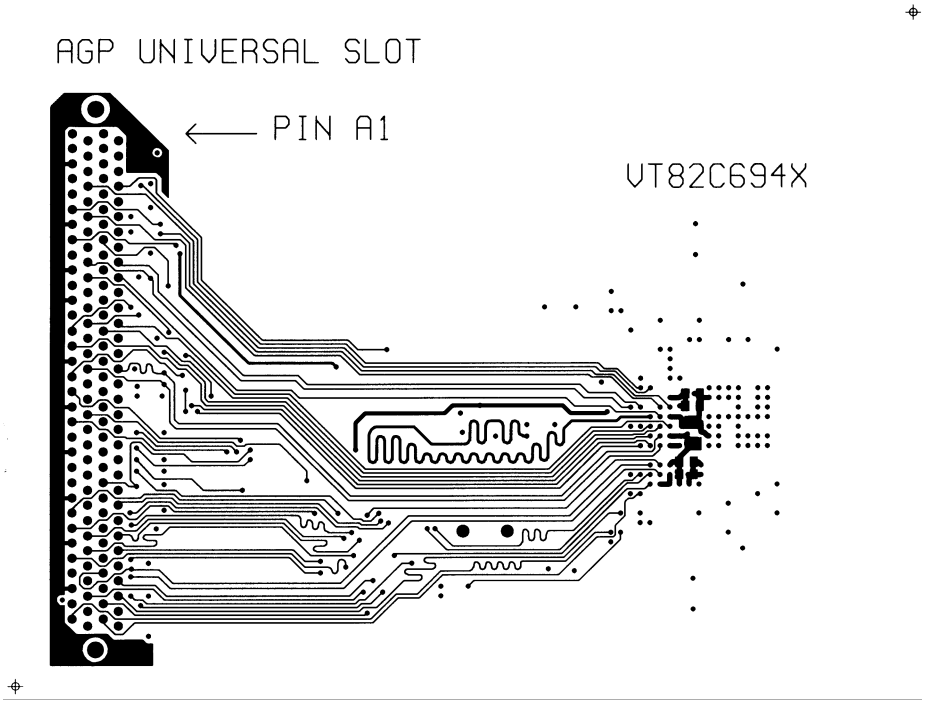
- An impedance of 65 ohm ± 5 ohm is strongly recommended for AGP 4X. Otherwise, signal integrity requirements may be violated.

- **Five extra decoupling capacitors is required for VDDQ power plane. These decoupling capacitors are mounted right beneath the inner AGP quadrant of BGA area on the solder layer. The combination of these decoupling capacitors is one 1uF in 1206 size, two 1uF capacitors in 0805 size, one 0.1uF capacitor in 0805 size and one 0.01uF capacitor in 0805 size.**

- AGP signals GREQ#, GGNT#, GFRAME#, GTRDY#, GIRDY#, GDEVSEL#, GSTOP#, GSERR#, GPERR#, GPAR, GRBF#, GPIPE#, GDS[1:0], SBS and GWBF# require discrete pull-up resistors (not R-packs) to be installed on the motherboard. These signals must be pulled up to VDDQ using 8.2K~10K ohm pull-up resistors. It is recommended to keep the stub length as short as possible. Similarly, AGP signals GDS0#, GDS1# and SBS# require discrete 8.2K~10K ohm pull-down resistors to be installed on the motherboard.



(a) Component Side



(b) Solder Side

Figure 2-50. AGP 4X Interface Layout Example

Notes:
1. *Most Decoupling capacitors are placed on the left-hand side of the AGP slot in Figure 2-50 (a).*
2. *Discrete pull-up resistors are located very near their associated pins for the short stub limitation in Figure 2-50 (a).*
3. *Each Strobe signal is centered within its group to minimize the signal to strobe skew.*
4. *The serpentine bold trace near the VT82C694X chip represents the AGP clock feedback (GCLKI) signal in Figure 2-50 (b).*
5. *There are five SMD ceramic capacitors located in the inner AGP quadrant of BGA area in Figure 2-50 (b).*
6. *In order to prevent couplings from or to other signal groups (e.g. PCI), a surrounding ground plane is applied near the AGP universal (2X or 4X) slot on either the component layer or the solder layer.*

2.4.4 PCI Interface Layout and Routing Guidelines

It is recommended that the VT82C694X and VT82C686A be placed at both ends of the PCI bus for better signal termination. A topology example of the AGP and PCI buses on an ATX form factor is shown in Figure 2-51 below. PCI signal traces may be placed on either the component layer or the solder layer. Most AGP signal traces should be placed on the component layer.

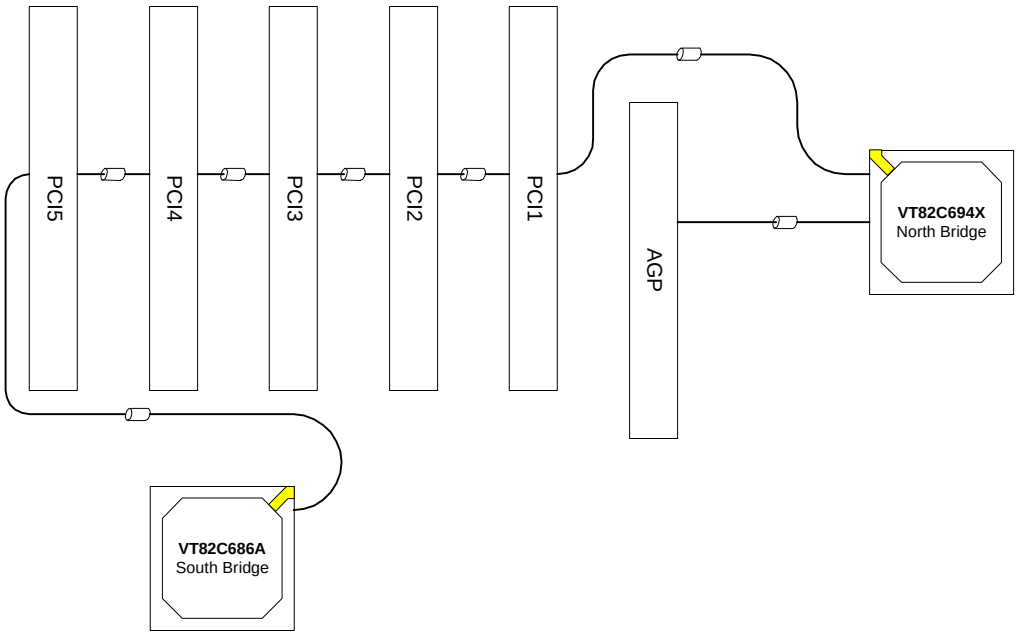


Figure 2-51. Topology Example of AGP and PCI Interface

Each of the following signals IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#, PERR#, SERR#, FRAME#, INTA#, INTB#, INTC#, and INTD# for the PCI interface requires a 4.7K ohm pull-up to VCC5. The REQ# signals need 2.2K ohm pull-ups to VCC5. The GNT# signals need 2.2K ohm pull-ups to VCC3.

The layout guidelines for PCI signals are listed below:

- Maintain 5 mil trace width and 10 mil clearance to its adjacent signals.
- Route to minimum trace length wherever possible.

2.5 Super South (VT82C686A) Layout and Routing Guidelines

2.5.1 USB controller

The Universal Serial Bus (USB) provides a bi-directional, isochronous, hot-attachable Plug and Play serial interface for adding external peripheral devices such as game controllers, communication devices, and input devices on a single bus. Brief descriptions of the USB signals of the VT82C686A are listed in Table 2-12. The VT82C686A provides four USB ports. Only port 0 and port 1 have over-current detect pins (OC0# and OC3#), however, the over current status of port 2 and port 3 can still be sensed for implementing 4 USB ports. The VT82C686A will scan SD[3:0] during the ISA refresh period as OC[3:0]# of the USB ports. If this over-current scan logic is implemented, pins OC0# and OC1# may be left open or used for alternative functions. A schematic drawing for four over-current scans is illustrated in Figure 2-52 below.

Table 2-12 Universal Serial Bus (USB) Signals

Signal Name	I/O	Description
USBP0+	IO	USB Port 0 Data +
USBP0-	IO	USB Port 0 Data -
OC0#	I	USB Port 0 Over Current Detect. Port 2 is disabled if this input is low.
USBP1+	IO	USB Port 1 Data +
USBP1-	IO	USB Port 1 Data -
OC1#	I	USB Port 1 Over Current Detect. Port 1 is disabled if this input is low.
USBP2+	IO	USB Port 2 Data +
USBP2-	IO	USB Port 2 Data -
USBP3+	IO	USB Port 3 Data +
USBP3-	IO	USB Port 3 Data -
USBCLK	I	USB clock. Connected to a 48MHz clock output of the system clock synthesizer.

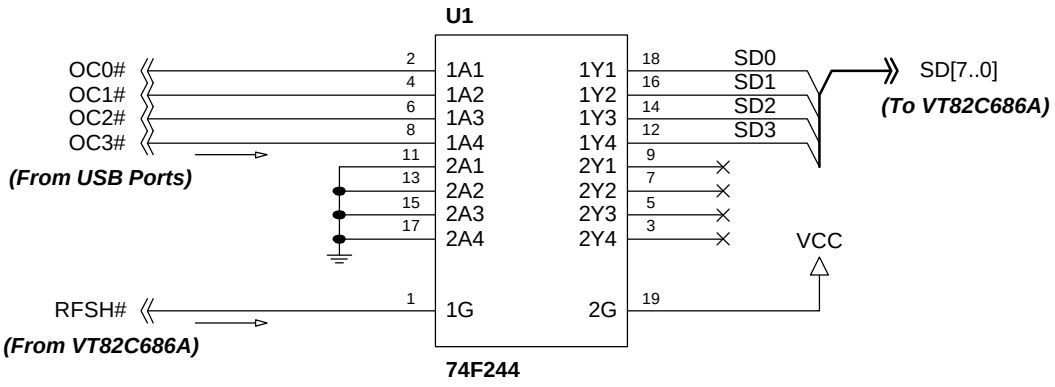


Figure 2-52. USB Over-Current Scan Logic

The layout guidelines for USB are listed below.

- Each pair of USB data signals is required to be parallel to each other with the same trace length.
- Each pair of USB data signals is required to be parallel to a respective ground plane.

A routing example of two pairs of USB data buses is shown in figure 2-53 below.

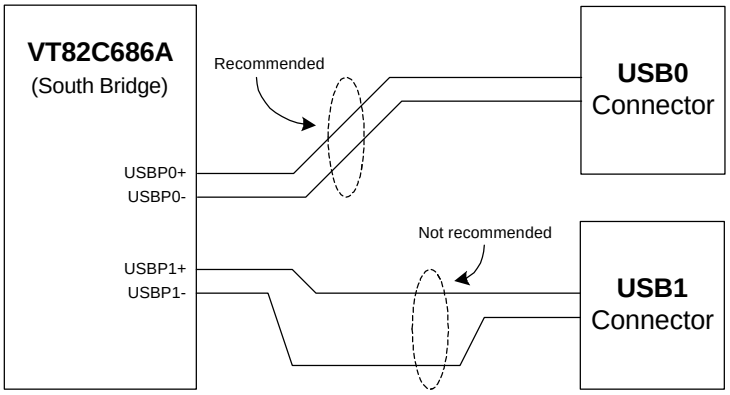


Figure 2-53. USB Differential Signal Routing Example

2.5.2 AC'97 Link and Game/MIDI Ports

Table 2-13 shows a brief description of the signals of AC'97 Link Controller and Game Ports. All those signals are multi-function pins with the second IDE channel bus. To enable both functions, the power up strapping of SPKR (pin V5 of the VT82C686A) must be pulled up to VCC3 with a 4.7K~10K ohm resistor.

Table 2-13. Signal Description of AC'97 Link and Game/MIDI Ports

Signal Name	I/O	Description
BITCLK (SDD0)	I	AC'97 Bit Clock
SDIN (SDD1)	I	AC'97 Serial Data In
SDIN2 (SDD2)	I	AC'97 Serial Data In 2 (reserved)
SYNC (SDD3)	O	AC'97 Sync
SDOUT (SDD4)	O	AC'97 Serial Data Out
ACRST (SDD5)	O	AC'97 Reset
JBY (SDD6)	I	Game Port Joystick B Y-axis
JBX (SDD7)	I	Game Port Joystick B X-axis
JAY (SDD8)	I	Game Port Joystick A Y-axis
JAX (SDD9)	I	Game Port Joystick A X-axis
JAB2 (SDD10)	I	Game Port Joystick A Button 2
JAB1 (SDD11)	I	Game Port Joystick A Button 1
JBB2 (SDD12)	I	Game Port Joystick B Button 2
JBB1 (SDD13)	I	Game Port Joystick B Button 1
MSO (SDD14)	O	MIDI Serial Out
MSI (SDD15)	I	MIDI Serial In

2.5.2.1 AC'97 Link

An AC'97 Controller is integrated in the VT82C686A and currently supports only one Codec. One Primary Codec (ID 00) is completely compatible with existing AC'97 definitions and extensions. The Codec ID functions as a chip set select. For more details, refer to the AC'97 Component Specification Revision 2.1.

AC-link is a digital serial link between the AC'97 Controller and AC'97 devices. AC-link signals are multi-function pins with the Second IDE channel bus (SDD[0..5]). A linking example between the AC'97 Controller and one AC'97 Codec is shown in figure 2-54. A complete schematic for implementing the VIA VT1611A AC'97 Audio Codec is shown in Appendix B.

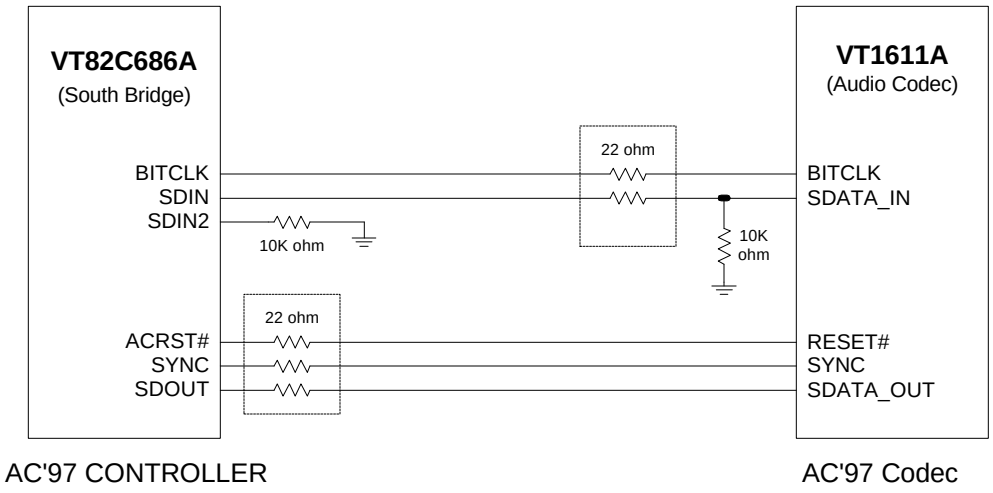


Figure 2-54. AC'97 Link Example

2.5.2.2 Game/MIDI ports

The VT82C686A supports two direct game ports (Joystick A and Joystick B) and one MIDI port interface. An application circuit of MIDI/Game port is shown in Figure 2-55. It is recommended to place all these RC components near the D-SUB connector.

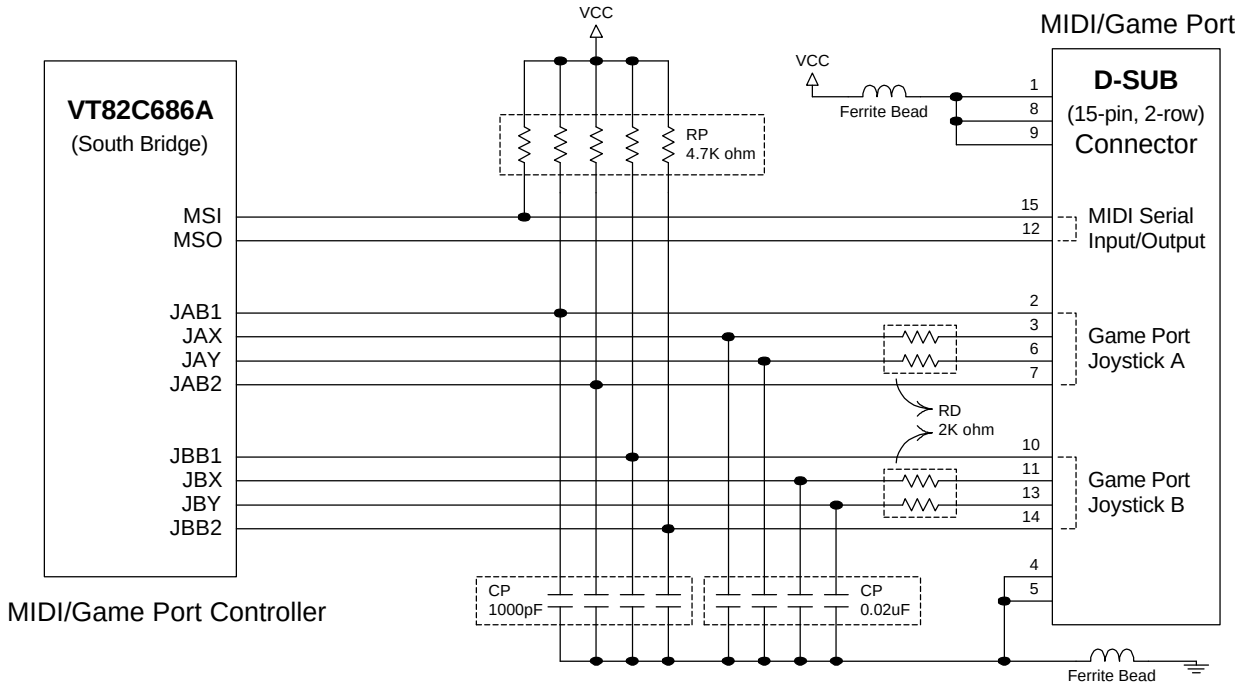


Figure 2-55. MIDI/Game Port Application Circuit

2.5.3 Hardware Monitoring

The hardware monitoring interface includes five positive voltage sensing inputs (four external and one internal), three temperature sensing inputs (two external and one internal), two fan-speed monitoring inputs and one chassis intrusion detection input. Programmable control, status, monitor and alarm are supported by the VT82C686A for flexible desktop management. The following sections provide detailed descriptions for each hardware monitor subsystem. An application circuit for hardware monitoring is shown in Figure 2.56. In order to achieve a stable VCC3 input to the Hardware Monitoring Subsystem, a 0.1uF decoupling capacitor should be placed as close to the Hardware Monitoring power and ground pins as possible.

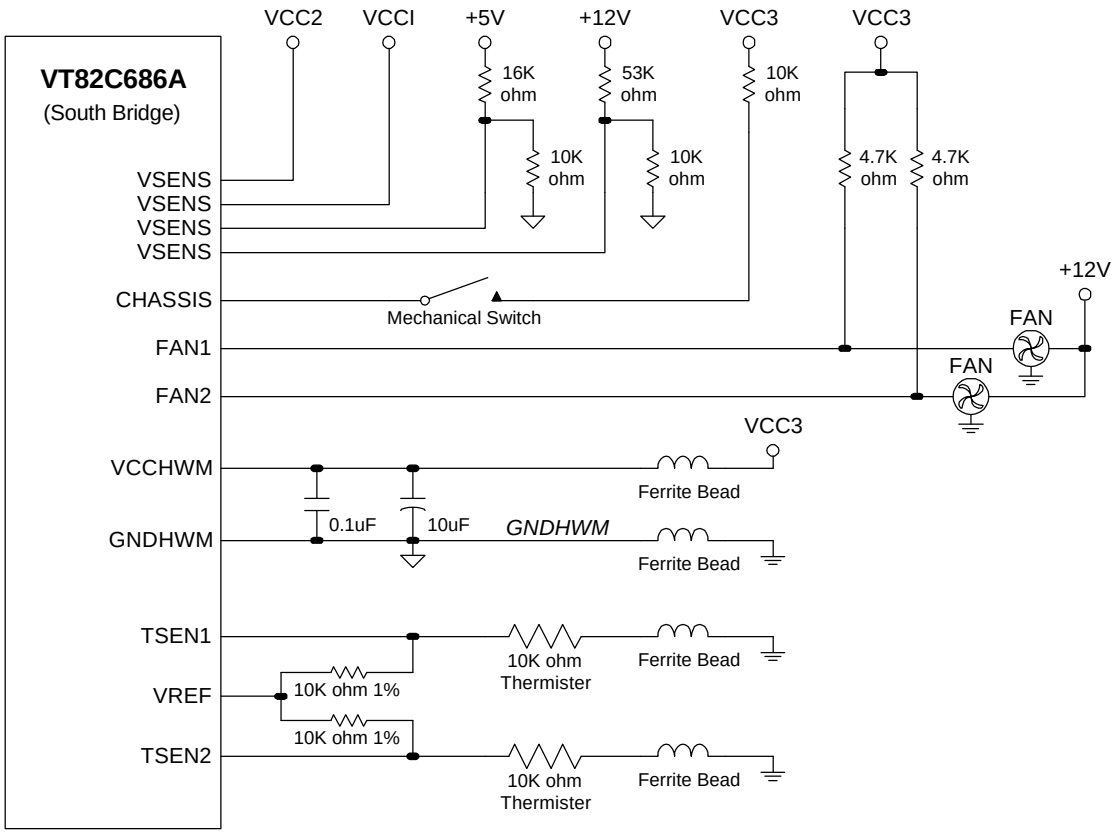


Figure 2-56. Hardware Monitoring Application Circuit

Voltage Monitoring

Typically VCC2 (core voltage of the CPU), VCCI (2.5V, core voltage of the VT82C694X), VCC3 (3.3V), 5V, and +12V are the five monitored voltage inputs. VCC2 and VCCI can be directly connected to the inputs. The +5V and 12V inputs should be attenuated with external resistors to any desired value within the input range. VCC3 is internally connected to the hardware monitoring system voltage detection circuitry for 3.3V monitoring. An alarm will issue when any monitored voltage level is out of range. Layout and grounding guidelines are listed below:

- These voltage inputs will provide better accuracy when referred to their respective ground (GNDHWM) which is separated from digital common ground (GND). Please refer to the application circuit above.
- Voltage dividers should be located physically as close to the voltage input pins as possible.

Temperature Sensing

One internal thermal sensor is located inside the VT82C686A chip. Two external thermisters for two temperature sensing inputs are used to directly contact the device whose temperature will be monitored. Layout and grounding guidelines are listed below:

- The thermister should be placed very near a measured object. For example, a thermister can be placed right beside of a Slot-1 CPU or under a Socket-370 CPU.
- The other end of a thermister should be connected to ground through a ferrite bead.

Fan-Speed Monitoring

Fan speed inputs are provided for signals from fans equipped with tachometer outputs. One fan-speed-monitoring pin can be used to measure the CPU fan speed. The other can be an auxiliary one. A programmable fan-speed control can be implemented in the following three steps.

- **Speed Monitoring:** The fan speed value is measured by a fan-speed monitoring pin
- **Temperature Sensing:** The temperature value is measured by a temperature sensing pin
- **Speed Controlling:** The fan speed is controlled by a dedicated General Purpose Output (GPO) pin

Chassis Intrusion Detection

The detection is an active high interrupt from any chassis intrusion violation. It could be accomplished mechanically, optically, or electrically. Circuitry external to the chassis intrusion detect pin is expected to latch the event.

2.5.4 Integrated Super IO Controller

In the VT82C686A, an integrated Super IO Controller supports two UARTs for complete serial ports, one dedicated IR port, one multi-mode parallel port, and one floppy drive controller function. Refer to the Apollo Pro-133 Reference Design Schematics in Appendix C for more details on application circuits.

2.5.5 System Management Bus Interface

The I2C bus signal pair of the VT82C686A will handle all I2C buses to other on-board devices such as the Clock Synthesizer and the three DIMM slots. A block diagram of System Management Bus Interfaces is shown in Figure 2-57. It is recommended to place both pull-ups at the end of the I2C bus.

- Adding 68pF capacitors in Figure 2-57 for the pair at the end device is essential since the I2C bus travels a long way and might pick up noise along the route.

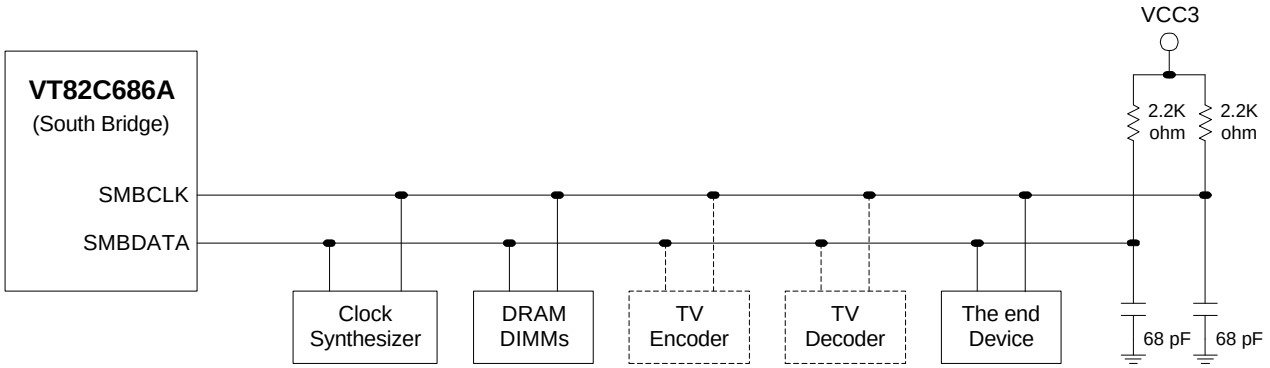
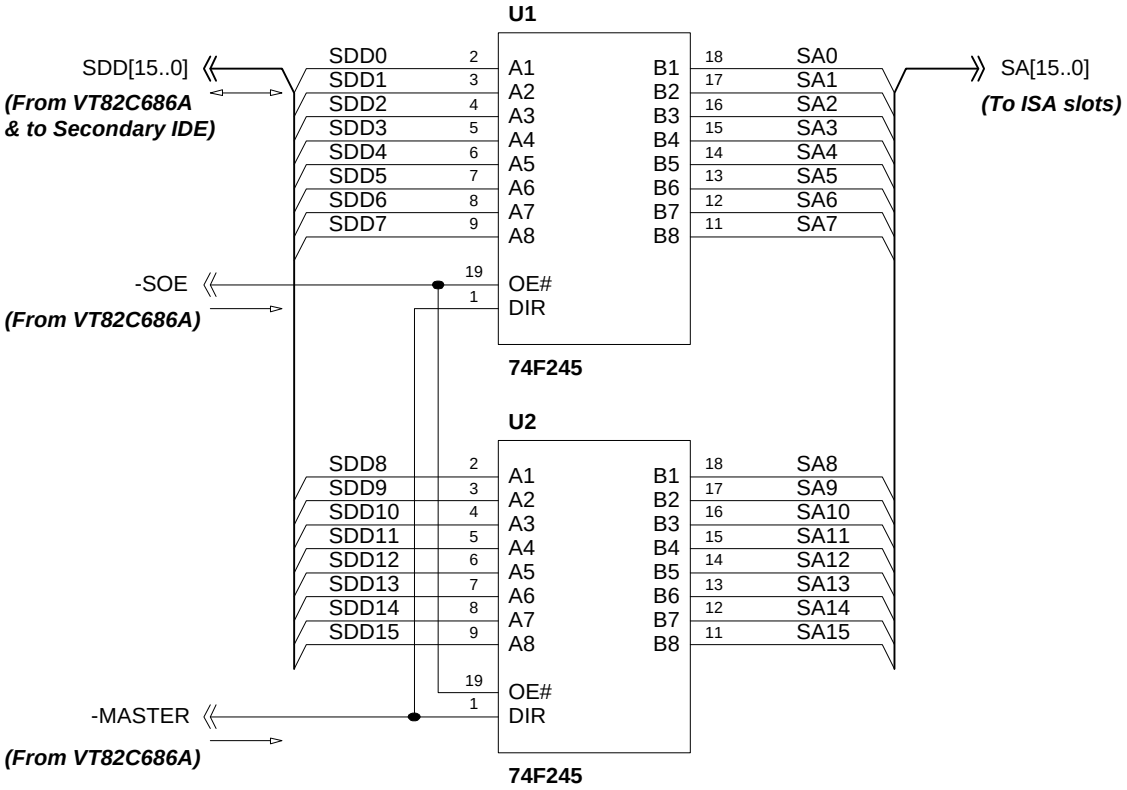


Figure 2-57. System Management Bus Interface

2.5.6 IDE

Both Primary and secondary IDE channels have their own control signals. The Primary IDE channel has a dedicated data bus. However, the secondary IDE data bus is multiplexed with an Audio/Game port or it can share ISA address bus SA[15:0] as SDD[15:0]. The two options are listed below for selecting the secondary IDE data bus.

- Option 1: The secondary IDE data bus uses its own bus SDD[15:0] sharing with an Audio/Game port when the SPKR pin is strapped low. No Audio/Game port is supported in this case since these functions are shared with the SDD[15..0] pins.
- Option 2: The secondary IDE data bus shares ISA address bus SA[15:0] as SDD[15:0] through two 74F245 transceivers when the SPKR pin is strapped high. The sharing circuitry is shown in Figure 2-58. Audio/Game port functions are enabled on the SDD[15:0] pins.

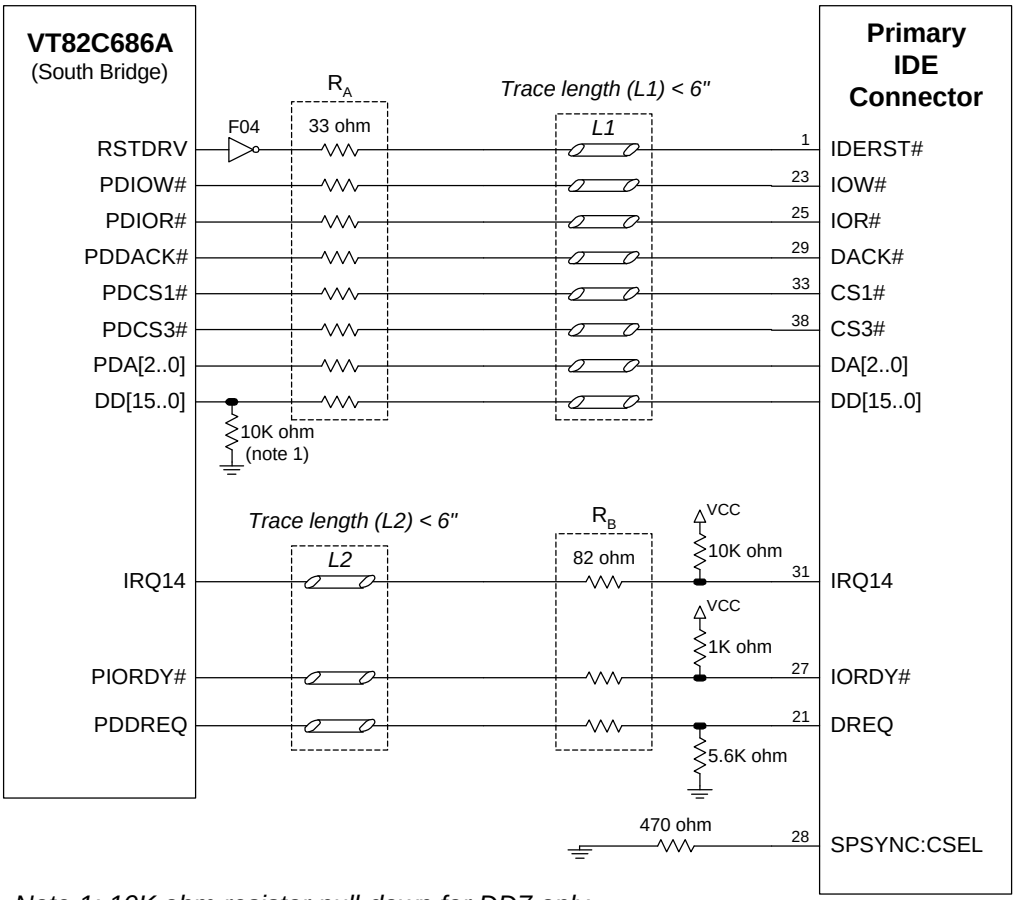


Note: These 74F245 Transceivers are optional if ISA bus load is not a concern.

Figure 2-58. ISA Bus SA[15:0] / SDD[15:0] Sharing Circuitry

Dual channel master mode PCI supports four Enhanced IDE devices. The transfer rate for each device can support up 33 MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-33 interface. Transmission line effects and signal crosstalk emerge in the IDE related signals. To eliminate ringing and reflection caused by the transmission line effect, trace length and impedance match must be taken into account. An example IDE layout is shown in Figure 2-59. Recommended layout rules for both primary and second IDE ports are listed below:

- The trace attribute of all primary IDE signals is in a minimum of 6 mils wide and 9 mils between two adjacent traces. The recommended trace length is less than 6 inches.
- All ATA signals in Figure 2-59 require series termination resistors. The series resistors (R_A) should be placed within 1 inch of the VT82C686A chip. The series resistors (R_B) should be placed within 1 inch of the primary IDE connector.
- Signal DD7 needs a 10K pull-down on the VT82C686A chip side of series termination
- Signal DREQ needs a 5.6K pull-down on the connector side of the series termination
- Signal IRQ14 (or IRQ15) needs a 10K pull-down or pull-up (preferred) on the connector side of the series termination
- Signal IORDY# needs a 1K pull-up on the connector side of the series termination
- Pin 28 of the IDE connectors should be tied to ground with a 470 ohm serial resistor.
- It is recommended to layout the following signals to each IDE connector in equal length. They are signals DD[15..0], IOR#, IOW#, and IORDY#.



Note 1: 10K ohm resistor pull-down for DD7 only

Figure 2-59. IDE Interfaces Layout Guidelines

Ultra DMA/66 Interface Layout Guidelines

VT82C686A supports Ultra DMA/66 IDE interfaces on both Primary IDE channel (IDE1) and Secondary IDE channel (IDE2). A Micro-ATX component placement example for implementing the Ultra DMA/66 interface (option 2) is shown in Figure 2-60. The detailed placement for the VT82C686A chip and two IDE connectors is illustrated in the lower left corner of the figure. The major difference from the former placement is the shorter distance between VT82C686A and primary IDE and Secondary IDE connectors. The shorter length for both IDE data buses is required because this bus is running at a high speed (66MHz). In order to fulfill this requirement, the VT82C686A chip can be lowered and both IDE connectors can be shifted to the left. Recommended layout guidelines are listed below.

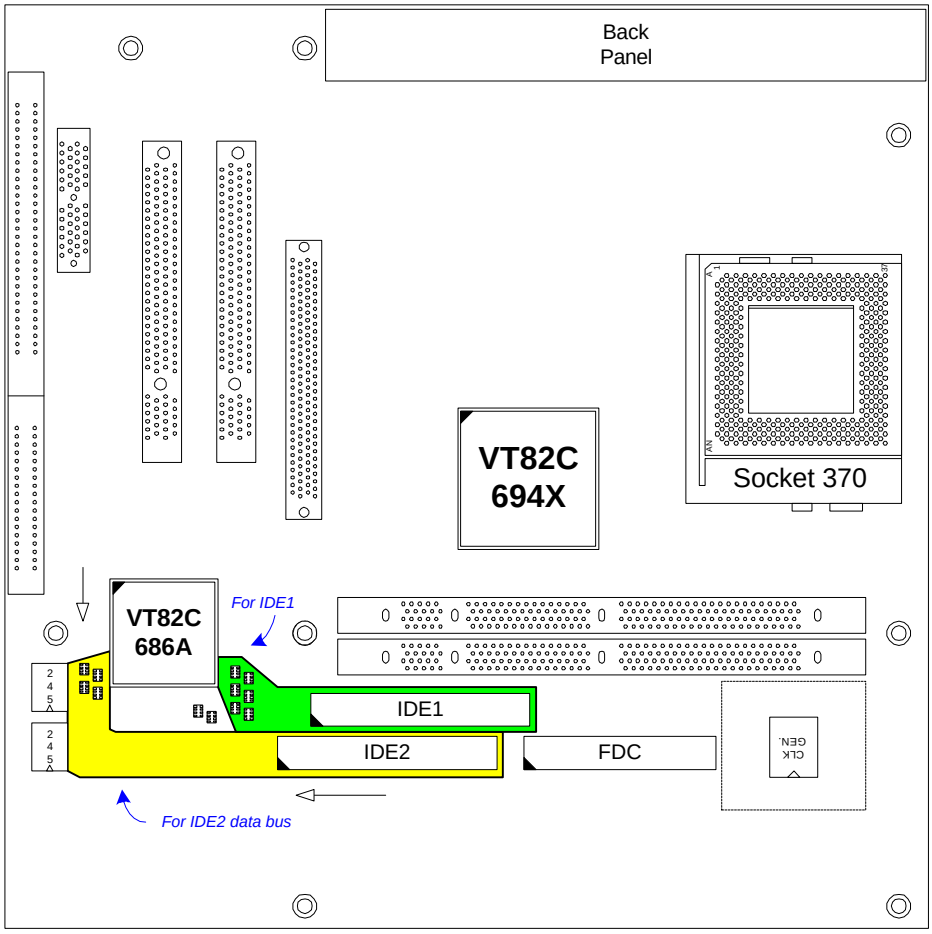
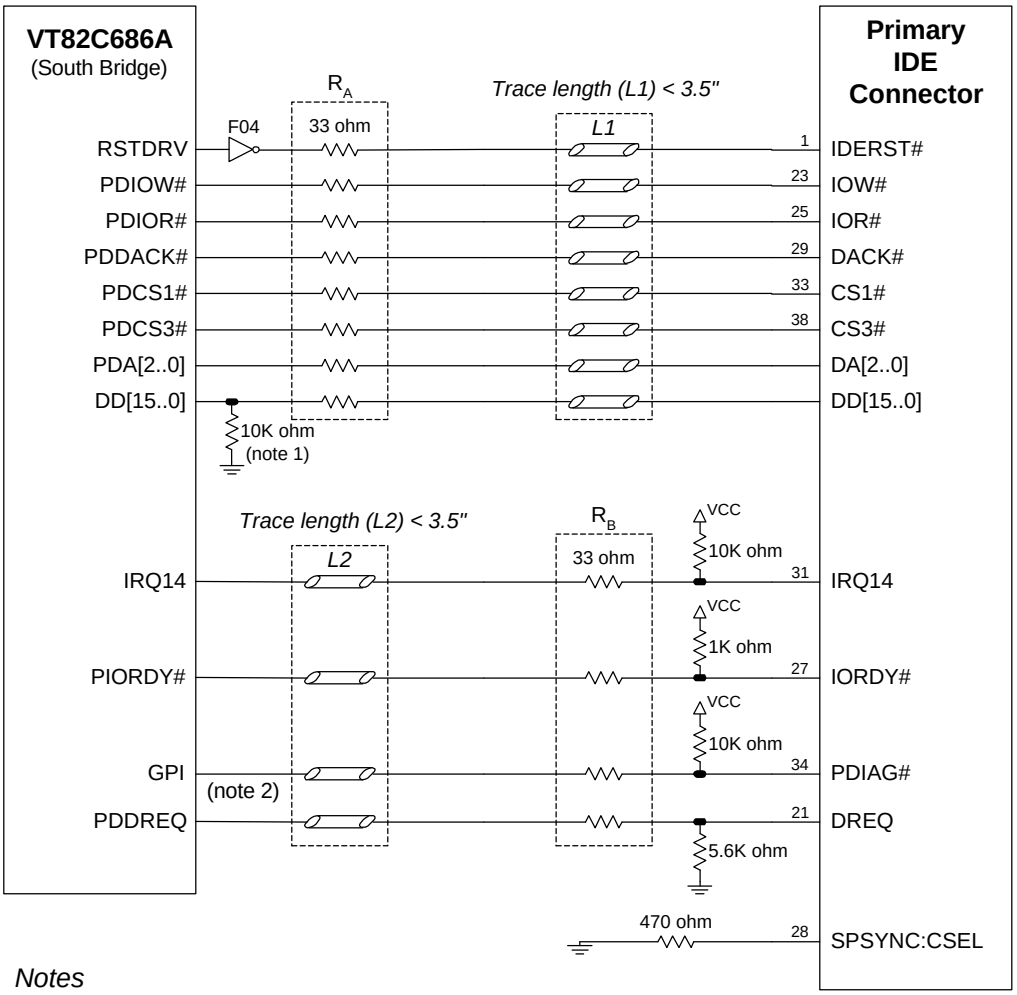


Figure 2-60. Ultra DMA/66 Placement and Routing Example

The application circuit of the ultra DMA/66 IDE interface is shown in Figure 2-61. The 80-conductor cable, required by the ultra DMA/66 IDE interface, is the major difference from the 40-conductor cable of the current IDE interface. For the detection of the 80-conductor cable, pin 34 (CBLID) of IDE connector may be used to provide a signal state from an ultra DMA/66 device to a GPI pin of the South Bridge Controller. The detection can be done in an alternative hardware solution too.

Layout rules for the IDE interface in the former section can be adapted for ultra DMA/66 use unless some of them are modified in the following layout guidelines.

- The trace attribute of all primary IDE signals is in a minimum of 6 mils wide and 9 mils between two adjacent traces.
- All signals for primary IDE and Secondary IDE require 33 ohm series termination resistors. Place these series terminations as close (less than 1 inch) to the VT82C686A as possible.
- Data and strobe lines should be routed as a bus. The total trace length of these signals should be shorter than 4.5 inches. The maximum trace length difference among them must be less than 1 inch. Other lines should be as short as possible.



Notes
1. 10K ohm resistor pull-down for DD7 only.
2. Pin 34 of primary IDE connector is connected to one of GPI pins from VT82C686A.

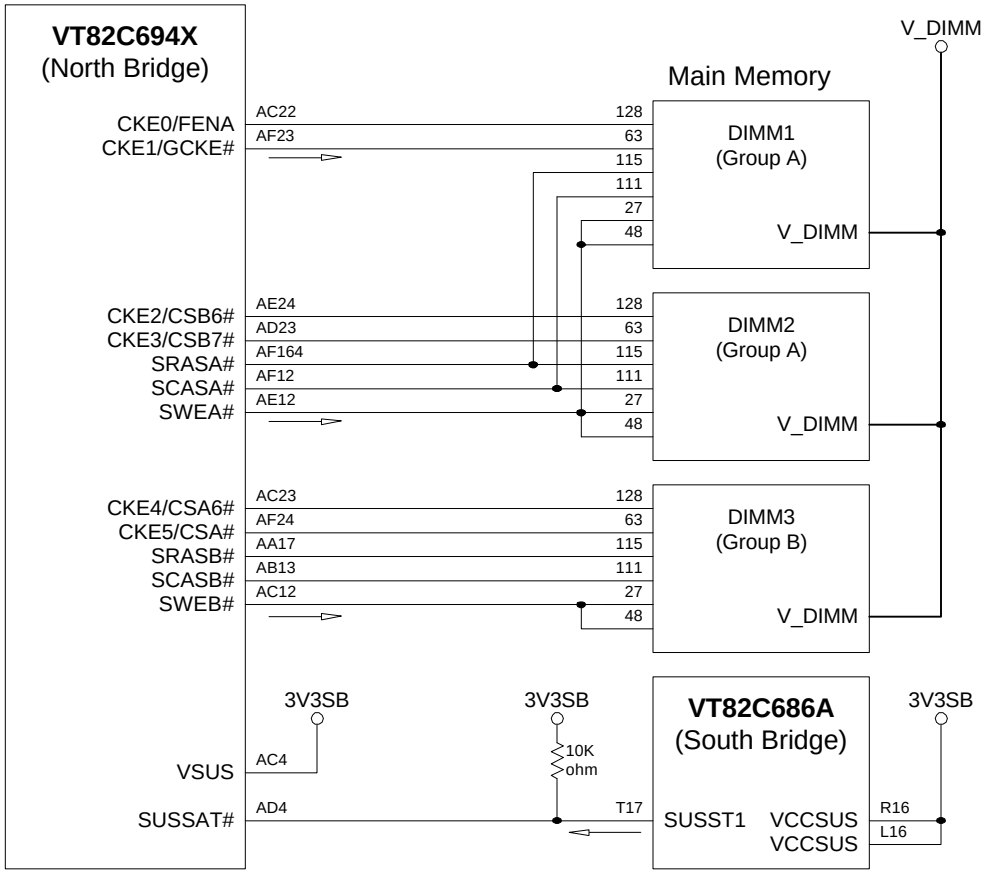
Figure 2-61. Ultra DMA/66 Application Circuit

2.5.7 Suspend to DRM

Power-on-suspend (POS), Suspend-to-RAM (STR) and Suspend-to-Disk (STD) or so called Soft-off are three different suspend states supported by the VT82C686A. These suspend functions are implemented not only in a notebook PC design but also in a desktop PC design. And the STR function is specially described in this section.

2.5.7.1 Suspend DRAM Refresh

During STR state, power is removed from most of the system except the system DRAM and the power management section of VT82C686A. Power is supplied to the suspend refresh logic of the VT82C694X (VSUS) and the suspend logic of the VT82C686A (VCCSUS). One additional suspend status indicator (SUSST1#) is provided to inform the north bridge and the rest of the system of the processor and system suspend states. SUSST1# is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode. SUSST1# is asserted when the system enters the suspend state or the processor enters the suspend (C3) state. SUSST1# is connected to the north bridge to switch between normal and suspend-DRAM-refresh modes The Suspend DRAM Refresh application circuit is shown in Figure 2-62.



Notes:
1. During STR state, all VT82C694X and VT82C686A signals are powered by 3.3V suspend power.
2. Main memory is also powered by 3.3V suspend power through V_DIMM.

Figure 2-62. Suspend DRAM Refresh Application Circuit

Suspend DRAM refresh state (self refresh mode for DRAM modules) is entered by having CKE[0:5], SRAS[A:B}#, SCAS[A:B]# held low with SW[A:B]# high at the rising edge of the SDRAM clock.

2.5.7.2 STR Power Plane Control

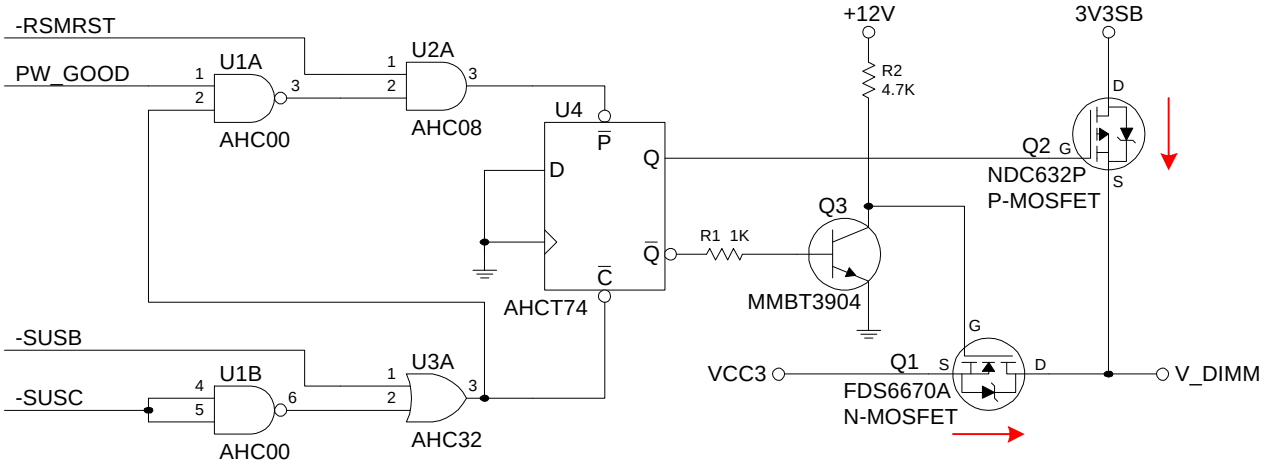
VT82C686A controls the system entering the various suspend states through the suspend control signals listed in Table 2-14. Three power plane control signals (SUSA#, SUSB# and SUSC#) are provided to turn off more system power planes as the system moves to deeper power-down states from normal operation to POS (only SUSA# asserted), to STR (both SUSA# and SUSB# asserted), and to STD (all three SUS# signals asserted).

Table 2-14. Resume Events Supported in Different Power States

Power State	RSMRST#	SUSST1#	SUSA#	SUSB#	SUSC#
On	1	0	1	1	1
POS	1	0	0	1	1
STR	1	0	0	0	1
STD / Soft-off	1	0	0	0	0
Mechanical off	0	0	0	0	0

Upon initiation of suspend, VT82C686A will assert the SUSST1# and SUS[A:C]# signals in a plane defined sequence to switch the system into the desired power state. The SUSA#, SUSB# and SUSC# signals can be used to control various power planes in the system. For example, SUSC# is typically connected to PS-ON (pin 14) of the ATX power supply connector through an inverter to control the remote-off function.

Figure 2-63 shows an application circuit example on STR power plane control. When SUSB# is not asserted, Q1 is turned on and Q2 is turned off. And V_DIMM power source is supplied by VCC3 in normal operation. When SUSB# is asserted, Q1 is turned off and Q2 is turned on. And V_DIMM power source is supplied by 3V3SB (3.3V suspend power) during STR state.



Notes:
1. Components U1, U2, U3 and U4 are powered by +5V standby power source.
2. V_DIMM represents the power source to DIMM modules.
*3. $R_{DS(ON)}$ of Q1 (N-channel MOSFET) should be as low as possible. RDS(ON)= **0.008 ohm** at VGS=10V for FDS6670A.*

Figure 2-63. STR State Power Plane Control Application Circuit

Note that these signals are associated with a particular type of suspend mode and power plane for descriptive purposes in this section. Using these signals, the system designer can control any type of function desired.

TIMING ANALYSIS AND SIMULATION

The 133 MHz timing analysis here will provide a basis for the concept of trace length limitation for some high speed buses and control signals such as the CPU address bus (A[31:3]). A brief analysis is given for each diagram. 133 MHz system frequency is assumed where one clock (1T) represents 7.5 ns. Reasons for the limited lengths of some signals (referring to Section 2.3) are described in the timing analyses.

3.1 SDRAM Timing

Timing diagrams for CPU Read from SDRAM and CPU Post Write to SDRAM are illustrated in Figures 3-1 and 3-2. Timing analyses for SDRAM read and write cycles are listed below:

- The clock skew between the CPU clock and the SDRAM clocks will affect the setup time and hold time of SDRAM command signals and MD[63..0] because the CPU reads or writes the data out of or into the SDRAM. Therefore, clock alignment between the CPU clock and the SDRAM clocks should be maintained.
- According to the cycles below, the timing is critical. In order to increase the timing margin of the cycle, one of the best solutions is to minimize the propagation delay of the MD[63..0] and SDRAM control signals on the PCB. Therefore, the length of MD[63..0] and the SDRAM control signals should be limited because there is only one clock between assertion of the SDRAM control signals and data input or output.

CCLK	**c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c**
ADS#	**h h f r h f r h f r h h h h h h h h h h h h h h h h h h h h h h h**
HREQ#	**z z n x o n x o n x o z z z z z z z z z z z z z z z z z z z z z z z**
HA#	**z z n x o n x o n x o z z z z z z z z z z z z z z z z z z z z z z z**
RS#	**z z z z z z z z z z n o z z n o z z n o z z z z z z z z z z z z z z**
DBSY#	**h h h h h h h h h h f l l r f l l r f l l r h h h h h h h h h h h h h**
DRDY#	**h h h h h h h h h h f l l l l l l l l l l r h h h h h h h h h h h h h**
HTRDY#	**h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h**
HD	**z z z z z z z z z z n x x x x x x x x x x o z z z z z z z z z z z z z**
CS#	**h h h h f r f r h h f r h h f r h h h h h h h h h h h h h h h h h h**
SRAS#	**h h h h f r h h h h h h h h h h h h h h h h h h h h h h h h h h h h**
SCAS#	**h h h h h h f r h h f r h h f r h h h h h h h h h h h h h h h h h h**
SWE#	**h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h h**
MD#	**z z z z z z z z z n x x x x x x x x x x o z z z z z z z z z z z z z**

Consideration:
A: Be careful of the MD data length
B: Be careful of the CPU data length
C: Be careful of the CPU address length
D: Be careful of the CPU control signal length

Figure 3-1. CPU Read from SDRAM (SL=2)

CCLK	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
ADS#	h	h	f	r	h	f	r	h	f	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
HREQ#	z	z	n	x	o	n	x	o	n	x	o	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z
HA#	z	z	n	x	o	n	x	o	n	x	o	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z
RS#	z	z	z	z	z	z	z	z	n	o	z	z	n	o	z	z	n	o	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z
DBSY#	h	h	h	h	h	h	h	f	l	l	r	f	l	l	r	f	l	l	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
DRDY#	h	h	h	h	h	h	h	f	l	l	l	l	l	l	l	l	l	l	l	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
HTRDY#	h	h	h	h	h	f	l	r	f	l	r	f	l	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
HD	z	z	z	z	z	z	z	n	x	x	x	x	x	x	x	x	x	x	x	o	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z	z
CS#	h	h	h	h	h	h	h	f	r	f	r	h	h	f	r	h	h	f	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
SRAS#	h	h	h	h	h	h	h	f	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
SCAS#	h	h	h	h	h	h	h	h	h	f	r	h	h	f	r	h	h	f	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
SWE#	h	h	h	h	h	h	h	h	h	f	r	h	h	f	r	h	h	f	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h	h
DQM#	h	h	h	h	h	h	h	h	h	f	l	l	l	l	l	l	l	l	l	l	l	r	h	h	h	h	h	h	h	h	h	h	h	h	h	h
MD#	z	z	z	z	z	z	z	z	z	n	x	x	x	x	x	x	x	x	x	x	x	o	z	z	z	z	z	z	z	z	z	z	z	z	z	z

Consideration:
A: Be careful of the MD data length
B: Be careful of the CPU data length
C: Be careful of the CPU address length
D: Be careful of the CPU control signal length

Figure 3-2. CPU Post Write to SDRAM (SL=2)

ELECTRICAL SPECIFICATIONS

This section describes the electrical specifications of the VT82C694X.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation is not implied under the ratings listed in Table 4-1.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_A	Ambient Operating Temperature	0	70	^{0}C	1
T_S	Storage Temperature	-55	125	^{0}C	1
V_{IN}	Input Voltage	-0.5	V_{RAIL} + 10%	Volts	1,2
V_{OUT}	Output Voltage	-0.5	V_{RAIL} + 10%	Volts	1,2

Notes:

1. *Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.*
2. *V_{RAIL} is defined as the VCC level of the respective rail. The CPU interface can be 3.3V or 1.5V. The Memory interfaces must be 3.3V only. The PCI and AGP interfaces can be 3.3V or 5.0V.*

4.2 Recommended Operating Ranges

Functional operation of the VT82C694X is guaranteed if the values of voltage and temperature are within the limits defined in Table 4-2.

Table 4-2. Recommended Operating Ranges

Symbol	Parameter	Min	Max	Notes
T_A	Ambient Operating Temperature	0 ^{0}C	70 ^{0}C	
V_{TT}	1.5V Power (GTL bus)	1.425 V	1.575 V	
V_{CC3}	3.3V Power to (IO Buffer)	3.135 V	3.465 V	
V_{CC5}	+5V Power	4.75 V	5.25 V	

4.3 DC Characteristics

DC characteristics of the VT82C694X are shown in Table 4-3.

Table 4-3. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	+2.0	V_{CC}+0.5	V	Note 1
V_{OL}	Output Low Voltage	-	0.45	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 1.0 mA
I_{IL}	Input Leakage Current	-	+/-10	uA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate Leakage Current	-	+/-20	uA	$0.45 < V_{OUT} < V_{CC}$
I_{CC1_5}	Power Supply Current (GTL)	-		mA	Note 2
I_{CC3}	Power Supply Current	-		mA	Note 3

Notes:
1. V_{CC} refers to the voltage being applied to VCC during functional operation.
2. V_{TT} = 1.5 V - The maximum power supply current must be taken into account when designing a power supply.
3. V_{CC3} = 3.3 V - The maximum power supply current must be taken into account when designing a power supply.

4.4 Power Dissipation

Table 4-4 contains the maximum power dissipation of the VT82C694X during different system frequencies.

Table 4-4. Maximum Power Dissipation

Supply Voltage	66MHz	100MHz	133MHz	Conditions
1.5V	W (V_{TT} = mA)	W (V_{TT} = mA)	W (V_{TT} = mA)	
3.3V	W (V_{CC3} = mA)	W (V_{CC3} = mA)	W (V_{CC3} = mA)	
Total power consumption	W	W	W	

SIGNAL CONNECTIVITY AND DESIGN CHECKLIST

5.1 Overview

The Apollo Pro133A North Bridge, and VT82C686A South Bridge are the two major components in a VIA Apollo Pro133A based PC system. Two signal connectivity tables for both North Bridge and South Bridge and a design checklist are given in the following sections. Pin connections may vary in different circuit designs. Some pins have been repeatedly described for different functions in different sub-tables.

The signal connectivity table provides board designers a quick reference of signal connections. And it can be used to review schematics of an Apollo Pro133A system. The design checklist can provide a quick way to review the PCB layout of an Apollo Pro133A system.

5.2 VT82C694X Apollo Pro133A North Bridge

The connectivity for each signal of the VT82C694X North Bridge is listed in Table 5-1. Motherboard designers can use this table as a quick reference to review their schematics.

Table 5-1. VT82C694X North Bridge Connectivity

CPU INTERFACE		
Signal Name	**I/O**	**Connection**
ADS#	IO (GTL+)	Connect to Slot-1 CPU. Or connected to Socket-370 CPU with 56 ohm termination to VTT.
BNR#	IO (GTL+)	Same as the above.
BPRI#	IO (GTL+)	Same as the above.
BREQ0#	O (GTL+)	Same as the above.
CPURST#	O (GTL+)	Same as the above.
DBSY#	IO (GTL+)	Same as the above.
DEFER#	IO (GTL+)	Same as the above.
DRDY#	IO (GTL+)	Same as the above.
HA[31:3]#	IO (GTL+)	Same as the above.
HD[63:0]#	IO (GTL+)	Same as the above.
HIT#	IO (GTL+)	Same as the above.
HITM#	I (GTL+)	Same as the above.
HLOCK#	I (GTL+)	Same as the above.
HREQ[4:0]#	IO (GTL+)	Same as the above.
HTRDY#	IO (GTL+)	Same as the above.
RS[2:0]#	IO (GTL+)	Same as the above.

DRAM INTERFACE		
Signal Name	**I/O**	**Connection**
MAA[14:0]	O	Connect to DIMM1 and DIMM2.
MAB[13:11]#, MAB10, MAB[9:0]#	O	Connect to DIMM3 for 3-DIMM case. Or connect to DIMM3 and DIMM4 for 4-DIMM case.
MD[63:0]	IO	Connect to each DIMM.
MECC[7:0]	IO	Same as the above.
RASA[5:0]# / CSA[5:0]#	O	Connect to DIMM1, DIMM2 and DIMM3. (two to each)
RASB[5:0]# / CSB[5:0]#	O	Same as the above.
CASA[7:0]# / DQMA[7:0]#	O	Connect to each DIMM.
CASB5# / DQMB5#	O	Connect to DIMM3 for 3-DIMM case. Or connect to DIMM3 and DIMM4 for 4-DIMM case.
CASB1# / DQMB1#	O	Same as the above.
SRASA#	O	Connect to DIMM1 and DIMM2.
SCASA#	O	Same as the above.
SWEA# / MWEA#	O	Same as the above.
SRASB#	O	Connect to DIMM3 for 3-DIMM case. Or connect to DIMM3 and DIMM4 for 4-DIMM case.
SCASB#	O	Same as the above.
SWEB# / MWEB#	O	Same as the above.
CKE[5:4] / CSA[7:6]#	O	CKE[5:4] connected to DIMM3 for 3-DIMM case. CSA[7:6]# connected to DIMM4 for 4-DIMM case.
CKE[3:2] / CSB[7:6]#	O	CKE[3:2] connected to DIMM2 for 3-DIMM case. CSB[7:6]# connected to DIMM4 for 4-DIMM case.
CKE1 / GCKE#	O	CKE1 connected to DIMM1 for 3-DIMM case.
CKE0 / FENA	O	CKE0 connected to DIMM1 for 3-DIMM case.

PCI BUS INTERFACE		
Signal Name	**I/O**	**Connection**
CBE[3:0]#	IO	Connect to VT82C686A and PCI slots.
AD[31:0]	IO	Same as the above.
FRAME#	IO	Connect between VT82C694X, PCI slots, and VT82C686A. 2.7K ohm pull-up to VCC5.
IRDY#	IO	Same as the above.
TRDY#	IO	Same as the above.
STOP#	IO	Same as the above.
DEVSEL#	IO	Same as the above.
SERR#	IO	Same as the above.
LOCK#	IO	Connect between VT82C694X and PCI slots. 2.7K ohm pull-up to VCC5.
PAR	IO	Connect to VT82C686A and PCI slots.
PREQ#	I	Connect to VT82C686A. 10K ohm pull-up to VCC3.
PGNT#	O	Connect to VT82C686A. 10K ohm pull-up to VCC3.
REQ[4:0]#	I	Connect to corresponding PCI slots. 2.7K ohm pull-up to VCC5.
GNT[4:0]#	O	Connect to corresponding PCI slots. 2.7K ohm pull-up to VCC3.
WSC#	O	No connect.

AGP BUS INTERFACE		
Signal Name	**I/O**	**Connection**
GBE[3:0]#	IO	Connect to AGP slot.
GD[31:0]	IO	Same as the above.
SBA[7:0]	I	Same as the above.
ST[2:0]	O	Same as the above.
GFRM#	IO	Connect to AGP slot. 8.2K ohm pull-up to VDDQ.
GIRDY#	IO	Same as the above.
GTRDY#	IO	Same as the above.
GSTOP#	IO	Same as the above.
GDSEL#	IO	Same as the above.
GDS0	IO	Same as the above.
GDS1	IO	Same as the above.
SBS	I	Same as the above.
GPIPE#	I	Same as the above.
GRBF#	I	Same as the above.
GREQ#	I	Same as the above.
GGNT#	O	Same as the above.
GGNT#	O	Same as the above.
GWBF#	I	Same as the above.
GDS0#	IO	Connect to AGP slot. 8.2K ohm pull-down to ground.
GDS1#	IO	Same as the above.
SBS#	I	Same as the above.
NCOMP	I	Connected to VDDQ through a 60 ohm resistor.
PCOMP	I	Connected to ground through a 60 ohm resistor.
GPAR / GCKRUN#	IO/O	Connect to AGP slot. Then connected to ground through a 100K ohm serial resistor.

CLOCK AND RESET CONTROL		
Signal Name	**I/O**	**Connection**
HCLK	I	Connect to the CPU clock output of the system clock synthesizer.
DCLKO	O	Connect to the SDRAM clock input of the system clock synthesizer.
DCLKWR	I	Connect to the SDRAM clock output of the system clock synthesizer.
GCLKO	O	Connected to the AGP clock input of the AGP slot through a 22 ohm resistor.
GCLK	I	Connected to the GCLKO of VT82C694X through a 22 ohm resistor.
PCLK	I	Connect to the PCI clock output of the system clock synthesizer.
RESET#	I	Connected to VT82C686A through a 74F240 inverter.
PWROK	I	Connect to VT82C686A and Power Good circuitry.
GCKRUN# / GPAR	O/IO	Connected to VT82C686A and the system clock synthesizer if the function is applied.
SUSCLK	I	Connect to VT82C686A. 10K ohm pull-up to VCC3.
SUSTAT#	I	Connect to VT82C686A. 10K ohm pull-up to VCC3.
CPURSTI#	I	Connect to the MUX circuitry of the CPU strapping signals. 10K ohm pull-up to VCC3.
CLKRUN#	I	Connected to VT82C686A and the system clock synthesizer if the function is applied. Otherwise, connect to VT82C686A then through a 100 ohm serial resistor to ground.

MISCELLANEOUS		
Signal Name	**I/O**	**Connection**
VCC	P	Connect to VCC3.
GND	P	Connect to ground.
VCCA	P	Connect to VCC3.
GNDA	P	Connect to ground.
VSUS	P	Connect to 3.3V standby power source.
VCCQ	P	Connect to VDDQ (1.5V or 3.3V).
VCCQQ	P	Connect to VDDQ (1.5V or 3.3V).
GNDQQ	P	Connect to ground.
VTT	P	Connect to GTL threshold voltage (1.5V).
GTLREF	P	Connect to GTL Buffer reference voltage (1.0V) circuitry.
AGPREF	P	Connect to AGP reference voltage (1.32V) circuitry.
TESTIN#	I	8.2K ohm pull-up to VCC3.

5.3 "Super South" South Bridge Controller

The connectivity for each signal of VT82C686A South Bridge is listed in Table 5-2. Motherboard designers can use this table as a quick reference to review their schematics. Some pins have been repeatedly described for different functions in different sub-tables, please be careful in using the following table.

Table 5-2. VT82C686A South Bridge Connectivity

PCI BUS INTERFACE		
Signal Name	**I/O**	**Connection**
PCLK	I	Connect to the PCI clock output of an external Clock Synthesizer.
AD[31:0]	IO	Connect to VT82C694X and PCI slots.
C/BE[3..0]#	IO	Connect to VT82C694X and PCI slots.
FRAME#	IO	Connect between VT82C694X, PCI slots, and VT82C686A. 10K ohm pull-up to VCC.
IRDY#	IO	Same as the above.
TRDY#	IO	Same as the above.
STOP#	IO	Same as the above.
DEVSEL#	IO	Same as the above.
SERR#	I	Same as the above.
PAR	IO	Connect to VT82C694X and PCI slots.
IDSEL	I	Connect to AD18 with a series 100 ohm resistor.
PIRQ[D:A]#	I	Connect to pins INT[D..A]# of each PCI slot as follows: PIRQA# PIRQB# PIRQC# PIRQD# PCI slot 1 INTA# INTB# INTC# INTD# PCI slot 2 INTB# INTC# INTD# INTA# PCI slot 3 INTC# INTD# INTA# INTB# PCI slot 4 INTD# INTA# INTB# INTC# Connect one of these pins to pin INTA# of VT82C694X.
PREQ#	O	Connect to VT82C694X.
PGNT#	I	Connect to VT82C694X.
PCKRUN#	IO	Connect to ground with a series 100 ohm resistor if the function is not applied.

CPU INTERFACE		
Signal Name	**I/O**	**Connection**
A20M#	OD	Connect to CPU. 4.7K ohm pull-up to VCC3.
CPURST	OD	Same as the above.
IGNNE#	OD	Same as the above.
INIT	OD	Same as the above.
INTR	OD	Same as the above.
NMI	OD	Same as the above.
SMI#	OD	Same as the above.
STPCLK#	OD	Same as the above.
FERR#	I	Same as the above.
SLP#/GPO7	OD	Connect to Slot-1 CPU only if the function is applied. 4.7K ohm pull-up to VCC3.

ISA BUS INTERFACE		
Signal Name	**I/O**	**Connection**
SA[19:16]	IO	Connect to ISA slots and BIOS ROM. 4.7K ohm pull-up to VCC. Connect SA[19:17] also to LA{19:17}.
SA[15:0]/SDD[15:0]	IO	Connect to ISA slots and BIOS ROM. 4.7K ohm pull-up to VCC. And connected to secondary IDE connector through two 74F245 ICs.
LA[23:20]	IO	Connect to ISA slots. 4.7K ohm pull-up to VCC.
SD[15:0]	IO	Connect to ISA slots and a 74F245 transceiver. 4.7K ohm pull-up to VCC.
SBHE#	IO	Connect to ISA slots. 4.7K ohm pull-up to VCC.
IOR#	IO	Same as the above.
IOW#	IO	Same as the above.
MEMR#	IO	Same as the above.
MEMW#	IO	Same as the above.
SMEMR#	O	Same as the above.
SMEMW	O	Same as the above.
BALE	O	Connect to ISA slots.
IOCS16#	I	Connect to ISA slots. 330 ohm pull-up to VCC.
MCS16#	I	Connect to ISA slots. 330 ohm pull-up to VCC.
IOCHCK#/GPI0	I	Connect to ISA slots. 4.7K ohm pull-up to VCC.
IOCHRDY	I	Connect to ISA slots. 4.7K ohm pull-up to VCC.
RFSH#	IO	Connect to ISA slots. 330 ohm pull-up to VCC.
AEN	O	Connect to ISA slots.
IRQ1/MSCK	I/IO	No connect.
IRQ[5:3]	I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ6/ GPI4/ SLPBTN#	I I I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ7	I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ8#/GPI1	I	No connect.
IRQ[11:9]	I	Connect to ISA slots. 4.7K ohm pull-up to VCC and 68pF capacitor to ground.
IRQ12/MSDT	I/IO	No connect.
IRQ[15:14]	I	Connect to ISA slots and IDE connectors. 4.7K ohm pull-up to VCC and 68pF capacitor to ground. Both passive components should be placed near the slots.
DRQ[1:0]	I	Connect to ISA slots. 5.6K ohm pull-down.
DRQ2/ SERIRQ/ GPIOE/ OC1#	I I IO I	Connect to ISA slots. 5.6K ohm pull-down.
DRQ3	I	Connect to ISA slots. 5.6K ohm pull-down.
DRQ[7:5]	I	Connect to ISA slots. 5.6K ohm pull-down.
DACK[1:0]#	O	Connect to ISA slots.
DACK2#/ GPIOF/ OC0#	I IO I	Connect to ISA slots.
DACK3#	I	Connect to ISA slots.
DACK[7:5]#	I	Connect to ISA slots.
TC	O	Connect to ISA slots. 68pF capacitor to ground
SPKR	O	Connected to speaker circuitry or AC'97 CODEC through a series 100 ohm resistor. 4.7K ohm pull-up to VCC3 for assigning SDD bus to Audio/Game or 4.7K ohm pull-down for unchanging SDD bus function.

USB INTERFACE		
Signal Name	**I/O**	**Connection**
USBP0+, USBP0-	IO	Connect to USB(0) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
OC0#/ DACK2#/ GPIOF	I I IO	Connect to the corresponding USB(0) over-current detection voltage divider.
USBP1+, USBP1-	IO	Connect to USB(1) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
OC1#/ DRQ2/ GPIOF/ SERIRQ	I I IO I	Connect to the corresponding USB(1) over-current detection voltage divider.
USBP2+, USBP2-	IO	Connect to USB(2) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
USBP3+, USBP3-	IO	Connect to USB(3) connector. 47pF capacitor to ground with 27 ohm resistor, and then 15K ohm resistor to ground. These passive components should be placed as close to VT82C686A as possible
USBCLK	I	Connect to a 48MHz clock output of the system clock synthesizer.

SYSTEM MANAGEMENT BUS INTERFACE		
Signal Name	**I/O**	**Connection**
SMBCLK, SMBDATA	IO	Connect to all devices on SMBus (I2C bus) except for the VGA port. 2.2K ohm pull-up to VCC3. This resistor value is varied based on the bus loading.
SMBALRT/GPI6	I	10K ohm pull-up to 3VSB (3.3V stand-by power source).

ULTRA DMA-66 ENHANCED IDE INTERFACE		
Signal Name	**I/O**	**Connection**
PDIOR#	O	Connected to primary IDE connector through a 33 ohm series resistor.
PDIOW#	O	Same as the above.
PDDACK#	O	Same as the above.
PDCS1#	O	Same as the above.
PDCS3#	O	Same as the above.
PDA[2:0]	O	Same as the above.
PDDRQ	I	Connected to primary IDE connector through a 33 ohm series resistor. 5.6K ohm pull-down on the connector side of the series resistor.
PDRDY#	I	Connected to primary IDE connector through a 33 ohm series resistor. 1K ohm pull-up to VCC on the connector side of the series resistor.
DD[15:0] /PDD[15:0]	IO	Connected to primary IDE connector through 33 ohm series resistors or also connected to secondary IDE connector through 33 ohm series resistors if SPKR is pulled up to VCC3. 10K ohm pull-down on the VT82C686A side of the series resistor.
SDIOR#	O	Connected to secondary IDE connector through a 33 ohm series resistor.
SDIOW#	O	Same as the above.
SDDACK#	O	Same as the above.
SDCS1#	O	Same as the above.
SDCS3#	O	Same as the above.
SDA[2:0]	O	Same as the above.
SDDRQ	I	Connected to secondary IDE connector through a 33 ohm series resistor. 5.6K ohm pull-down on the connector side of the series resistor.
SDRDY#	I	Connected to secondary IDE connector through a 33 ohm series resistor. 1K ohm pull-up to VCC on the connector side of the series resistor.
SDD15/MSI **SDD14**/MSO **SDD13**/JBB1 **SDD12**/JBB2 **SDD11**/JAB1 **SDD10**/JAB2 **SDD9**/JAX **SDD8**/JAY **SDD7**/JBX **SDD6**/JBY **SDD5**/ACRST **SDD4**/SDOUT **SDD3**/SYNC **SDD2**/SDIN2 **SDD1**/SDIN **SDD0**/BITCLK	IO/I IO/O IO/I IO/I IO/I IO/I IO/I IO/I IO/I IO/I IO/O IO/O IO/O IO/I IO/I IO/I	Connected to secondary IDE connector through 33 ohm series resistors when pin SPEAK is strapped to low. Otherwise, Connected to Audio/Game port instead when pin SPEAK is strapped to high.

PARALLEL PORT INTERFACE		
Signal Name	**I/O**	**Connection**
PD[7:0]	IO	Connect to the printer connector. 4.7K ohm pull-up to VCC and a 180pF decoupling capacitor to ground. These passive components should be placed near the connector.
AUTOFD#	IO	Same as the above.
PINIT#	IO	Same as the above.
SLCTIN#	IO	Same as the above.
STROBE#	IO	Same as the above.
ACK#	I	Same as the above.
BUSY	I	Same as the above.
ERROR#	I	Same as the above.
PE	I	Same as the above.
SLCT	I	Same as the above.

FLOPPY DISK INTERFACE		
Signal Name	**I/O**	**Connection**
DRVEN0	OD	Connect to primary floppy drive connector.
DRVEN1	OD	Connect to secondary floppy drive connector if it is installed. Otherwise, no connect.
DIR#	OD	Connect to the floppy drive connector.
DS0#	OD	Same as the above.
DS1#	OD	Same as the above.
HDSEL#	OD	Same as the above.
MTR0#	OD	Same as the above.
MTR1#	OD	Same as the above.
STEP#	OD	Same as the above.
WDATA	OD	Same as the above.
WGATE#	OD	Same as the above.
DSKCHG#	I	Connect to the floppy drive connector. 1K ohm pull-up to VCC.
INDEX#	I	Same as the above.
RDATA#	I	Same as the above.
TRK00#	I	Same as the above.
WRTPRT#	I	Same as the above.

SERIAL PORTS AND INFRARED INTERFACE		
Signal Name	**I/O**	**Connection**
TXD1	O	Connected to a corresponding 9-pin serial connector (usually COM1) through a serial RS232 interface buffer and a 330pF decoupling capacitor to ground.
RXD1	I	Same as the above.
RTS1#	O	Same as the above.
CTS1#	I	Same as the above.
DTR1#	O	Same as the above.
DSR1#	I	Same as the above.
DCD1#	I	Same as the above.
RI1#	I	Same as the above.
TXD2	O	Connected to a corresponding 9-pin serial connector (usually COM2) through a serial RS232 interface buffer and a 330pF decoupling capacitor to ground.
RXD2	I	Same as the above.
RTS2#	O	Same as the above.
CTS2#	I	Same as the above.
DTR2#	O	Same as the above.
DSR2#	I	Same as the above.
DCD2#	I	Same as the above.
RI2#	I	Same as the above.
IRTX/GPO14	O	Connect to an Infrared connector. 4.7K ohm pull-up to VCC.
IRRX/GPO15	IO	Connect to an Infrared connector.

SERIAL IRQ		
Signal Name	**I/O**	**Connection**
SERIRQ/ GPIOE/ OC1# DRQ2	I IO I I	4.7K ohm pull-up to VCC3.

INTERNAL KEYBOARD CONTROLLER		
Signal Name	**I/O**	**Connection**
KBCK/A20GATE	IO/I	Connected to a keyboard connector through a 4.7K ohm pull-up to VCC, a 47pF capacitor to ground, and a series ferrite bead.
KBDT/KBRC	IO/I	Same as the above.
MSCK/IRQ1	IO/I	Connected to a mouse connector through a 4.7K ohm pull-up to VCC, a 47pF capacitor to ground, and a series ferrite bead.
MSDT/IRQ12	IO/I	Same as the above.

GENERAL PURPOSE INPUTS		
Signal Name	**I/O**	**Connection**
GPI0/IOCHCK#	I	4.7K ohm pull-up to VCC3 if no multiplexed function is applied.
GPI1/IRQ8#	I	10K ohm pull-up to 3VSB if its function is applied. Same, if not applied.
GPI2/BATLOW#	I	4.7K ohm pull-up to VCC3 if no multiplexed function is applied.
GPI3/LID	I	Same as the above.
GPI4/IRQ6/ SLPBTN#	I	Same as the above.
GPI5/PME#/THRM	I	Same as the above.
GPI6/SMBALRT#	I	Same as the above.
GPI7/RING#	I	Same as the above.
GPI8/GPO8/GPIOA/G POWE#	IO	Same as the above.
GPI9/GPO9/GPIOB/ FAN2	IO	Same as the above.
GPI10/GPO10/GPIOC/ CHAS	IO	Same as the above.
GPI11/GPO11/ GPIOD	IO	Same as the above.

GENERAL PURPOSE OUTPUTS		
Signal Name	**I/O**	**Connection**
GPO0	O	10K ohm pull-up to 3VSB if its function is applied. Otherwise, no connect.
GPO1/SUSA#	IO	No connect if no multiplexed function is applied.
GPO2/SUSB#	IO	Same as the above.
GPO3/SDD2/SDIN2	O	Same as the above.
GPO4/CPUSTP#	O	Same as the above.
GPO5/PCISTP#	O	Same as the above.
GPO6/SUSST1#	O	Same as the above.
GPO7/SLP#	IO	Same as the above.
GPO8/GP18/GPIOA/ GPOWE#	IO	Same as the above.
GPO9/GPI9/GPIOB/ FAN2	IO	Same as the above.
GPO10/GPI10/GPIOC/ CHAS	IO	Same as the above.
GPO11/GPI11/GPIOD	IO	Same as the above.
GPO12/XDIR/PCS0#	O	Same as the above.
GPO13/SOE#/MCCS#	O	Same as the above.
GPO14/IRTX	O	Same as the above.
GPO15/IRRX	IO	Same as the above.
GPOWE#/GPIOA/ GPIO8	IO	Same as the above.

GENERAL PURPOSE I/O		
Signal Name	**I/O**	**Connection**
GPIOA(GPIO8)	IO	4.7K ohm pull-up to VCC3 if no multiplexed function is applied.
GPIOB(GPIO9)/FAN2	IO	Same as the above.
GPIOC(GPIO10)/ CHAS	IO	Same as the above.
GPIOD(GPIO11)	IO	Same as the above.
GPIOE/ OC1/ SERIRQ/ DRQ2	IO I I I	Same as the above.
GPIOF/ OC0/ DACK2#	IO I I	Same as the above.

HARDWARE MONITORING		
Signal Name	**I/O**	**Connection**
VSENS1	I	Connected to a monitored voltage (usually VCC2) through a voltage divider circuitry.
VSENS2	I	Connected to a monitored voltage (usually 2.5V) through a voltage divider circuitry.
VSENS3	I	Connected to a monitored voltage (usually VCC) through a voltage divider circuitry.
VSENS4	I	Connected to a monitored voltage (usually +12V) through a voltage divider circuitry.
TMPSENS1	I	Connect to a thermister that is near the sensed component or device.
TMPSENS2	I	Same as the above.
VREF	P	Connected to each thermister through a 10K ohm (1%) series resistor.
FAN1	I	Connect to a fan tachometer output
FAN2/GPIOB(GPIO9)	IO	Same as the above.
CHAS/GPIOC(GPIO10)	IO	Connect to chassis intrusion circuitry.

XD INTERFACE		
Signal Name	**I/O**	**Connection**
XDIR/PCS0#/GPO12	O	Connect to the direction control of a 74F245 transceiver that buffers the X-Bus data and ISA Bus data.
SOE#/MCCS#/GPO13	O	Connect to the output enable control of two 74F245 transceivers that buffers the secondary IDE data bus data and ISA address bus when the audio function is enabled.

CHIP SELECTS		
Signal Name	**I/O**	**Connection**
PCS0#/GPO12/XDIR	**O**	Connect to addressed devices which drive data to the SD pins if XDIR and SOE# are disabled and the X-Bus is not implemented.
MCCS#/GPO13/ SOE#	**O**	Connect to the chip enable control of a micro-controller chip if XDIR and SOE# are disabled and the X-Bus is not implemented.
ROMCS#/KBCS#	**O**	Connect to the chip enable control of BIOS ROM. 4.7K ohm pull-down for Socket-7 configuration or 4.7K ohm pull-up to VCC3 for Slot-1 configuration.

POWER MANAGEMENT		
Signal Name	**I/O**	**Connection**
PME#/THRM/GPI5	**I**	10K ohm pull-up to 3VSB if the function is not applied.
PWRBTN#	**I**	Connect to Power Button circuitry.
SLPBTN#/IRQ6/GPI4	**I**	10K ohm pull-up to VCC3 if the function is not applied.
RSMRST	**I**	Connect to Resume Reset circuitry.
EXTSMI#	**IOD**	10K ohm pull-up to 3VSB if the function is not applied.
SMBALRT#/GPI6	**I**	10K ohm pull-up to 3VSB if the function is not applied.
LID/GP13	**I**	10K ohm pull-up to 3VSB if the function is not applied.
RING#/GP17	**I**	Connected to external modem circuitry to allow the system to be re-activated by a received phone call. 10K ohm pull-up to 3VSB.
BATLOW#/GP12	I	10K ohm pull-up to 3VSB if the function is not applied.
CPUSTP#/GPO4	**O**	Connect to the system clock synthesizer to disable the CPU clock outputs if the function is applied. Otherwise, no connect.
PCISTP#/GPO5	**O**	Connect to the system clock synthesizer to disable the PCI clock outputs if the function is applied. Otherwise, no connect.
SUSA#/GPO1	**O**	10K ohm pull-up to 3VSB if the function is not applied.
SUSB#/GPO2	**O**	10K ohm pull-up to 3VSB if the function is not applied.
SUSC#	**O**	Connect to ATX Power On circuitry.
SUSST1#/GPO6	**O**	Connect to VT82C694X. 10K ohm pull-up to 3VSB.
SUSCLK	**O**	10K ohm pull-up to 3VSB

RESET AND CLOCKS		
Signal Name	**I/O**	**Connection**
PWRGD	I	Connect to VT82C694X and Power Good circuitry.
PCIRST#	O	Connect to PCI slots and PCI devices.
RSTDRV	O	Connected to VT82C694X and IDE connectors through a 74F240 inverter IC. And direct connect to ISA slots not through inverter.
OSC	I	Connect to the 14.318MHz clock output of the system clock synthesizer.
BCLK	O	Connected to ISA slots through corresponding 33 ohm series resistors.
RTCX1	I	Connect to a 32.768KHz (RTC) crystal circuitry.
RTCX2	O	Connect to a 32.768KHz (RTC) crystal circuitry.

POWER AND GROUND		
Signal Name	**I/O**	**Connection**
VCC	P	Connect to VCC3.
VCCSUS	P	Connect to 3VSB.
VCCHWM	P	Connected to VCC3 through a ferrite bead.
GNDHWM	P	Connected to ground through a ferrite bead.
VCCUSB	P	Connected to VCC3 through a ferrite bead.
GNDUSB	P	Connected to ground through a ferrite bead.
VBAT	P	Connect to battery circuitry.
GND	P	Connect to digital ground

5.4 Apollo Pro-133A Design Checklist

This Apollo Pro-133A (VT82C694X and VT82C686A) design checklist provides six checkup lists as a brief layout reference for implementing most layout requirements.

5.4.1 General Layout Considerations Checklist

For most signal traces on an Apollo Pro133A motherboard layout, 5-mil trace width and 10-mil spacing are advised. To reduce trace inductance, minimum power trace width is set at 30 mils. As a quick reference, recommended trace width and spacing for different trace types are listed in Table 5-3.

Table 5-3. Recommended Trace Width and Spacing

Trace Type	Trace Width (mils)	Spacing (mils)
Signal	5 or wider	10 or wider
Clock	15 or wider	15 or wider
Power	30 or wider	20 or wider

In high-speed bus design, general rules for minimizing crosswalk are listed below:

- Maximize the distance between traces. Maintain a minimum 10 mils space between traces wherever possible.
- Avoid parallelism between traces on adjacent layers.
- Select a board stack-up that minimizes coupling between adjacent traces.
- The recommended impedance should be in the range of 65 ohm +/- 5 ohm.

5.4.2 Major Components Checklist

Major components for the Apollo Pro-133A based system are listed below:

- Processor selection: Single Slot-1 CPU or Single Socket-370 CPU
- Apollo Pro-133 A chipset combination: VT82C694X and VT82C686A
- Apollo Pro-133A dedicate system clock synthesizers: ICS9248-39, PLL52C66-23 or IC Works W144
- Maximum DRAM DIMM slots: 4 (Maximum 8 banks up to 2GB DRAM)
- Maximum AGP slot: 1 only
- Maximum PCI slots: 5

5.4.3 Decoupling Recommendations Checklist

The high frequency and bulk decoupling capacitor distributions for major components are described in this section. Here, the high frequency decoupling capacitors include 0.1uF (0603), 1uF (0805) and 4.7uF (1206) SMD ceramic capacitors. The bulk decoupling capacitors include 10uF, 100uF and 1000uF electrolytic capacitors. The amount of bulk capacitors listed below is used as reference. More capacitor distributions are recommended. These decoupling capacitors should be located as close to the associated power and ground pins as possible.

For Slot-1 CPU, the decoupling capacitor requirements are listed below:

- VCC_CORE: 0.1uF x 9, 1uF x 10 and 1000uF x 6
- VTT: 0.1uF x 1, 1uF x1 and 100uF x 1
- VCC3: 0.1uF x 2, 1uF x 2 and 1000uF x 2
- VCC5: 0.1uF x 1, 1uF x 1

For Socket-370 CPU, the decoupling capacitor requirements are listed below:

- VCC_CORE: 0.1uF x 21, 1uF x 23, 4.7uF x 10 and 1000uF x 6
- VCC15: 0.1uF x 1, 1uF x1 and 1000uF x 4
- VREF: 0.1uF x 6, 1uF x 2 and 10uF x 1
- VCC25: 0.1uF x 1, 1uF x 1
- VCCCOMS: 0.1uF x 1, 1uF x 1

For Chipsets, the decoupling capacitor requirements are listed below:

- VT82C694X: 0.1uF x 8 or 1uF x 8
- VT82C686A: 0.1uF x 8 or 1uF x 8

For DIMM modules, the decoupling capacitor requirements are listed below:

- Two DIMM modules: 0.1uF x 9, 1uF x 10 and 1000uF x 2
- Three DIMM modules: 0.1uF x 12, 1uF x 15 and 1000uF x 4
- Four DIMM modules: 0.1uF x 16, 1uF x 20 and 1000uF x 5

For AGP slot, the decoupling capacitor requirements are listed below:

- +12V: 0.1uF x 1, 1uF x 1 and 10uF x 1
- VCC5: 0.1uF x 2, 1uF x 2 and 10uF x 1
- VCC3: 0.1uF x 9, 1uF x 9 and 1000uF x 1
- VDDQ (1.5V or 3.3V): 0.1uF x 11, 1uF x 11 and 1000uF x 2

Note: The capacitor of adjusting the SDRAM clock skew should be placed very near the ball AD25 (DCLKWR) of VT82C694X. Its capacitance is dependent on the SDRAM clock layout.

5.4.4 Clock Trace Checklist

The general clock routing guidelines are listed below:

- The recommended range of a clock trace width is between 15 mils and 20 mils.
- The minimum space between one clock trace and adjacent clock traces is 15 mils. The minimum space from one segment of a clock trace to other segments of the same clock trace is two times of the clock width. That is, more space is needed from one clock trace to others or its own trace to avoid signal coupling.
- Clock traces should be parallel to their reference ground planes. That is, a clock trace should be right beneath or on top of its reference ground plane.
- Series terminations (damping resistors) are needed for all clock signals (typically 10 ohms to 33 ohms). When two loads are driven by one clock signal, separate series terminations are required. When multiple loads (more than two) are applied, a clock buffer solution is preferred.
- Isolating clock synthesizer power and ground planes through ferrite beads or narrow channels (typically 20 mils to 50 mils) are preferred.
- No clock traces on the internal layer if a six-layer board is used.

5.4.5 Clock Trace Length Calculation

The trace length calculations for different clock signal groups are described in this section. A different component placement may result in a different calculation for the clock trace length. The trace length of those clock signals not mentioned in this section should be as short as possible or less than 9 inches.

CPU Clock Trace Length Calculation for Slot-1 System

Before routing any other signals on the board, pre-route every CPU clock trace from the system clock synthesizer to the Slot-1 CPU (CPUCLK) and North Bridge (HCLK) as short as possible. All high frequency clock alignment will be on the basis of the longest one (usually CPUCLK). A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → CPU	L_{CPU}	**L_{CPU}**	-	1"~9"
Clock chip → VT82C694X (NB)	L_{NB}	**L_{CPU} + 3"**	0.5"	4"~12"

Note: Here, the 3" represents the estimated trace length added into HCLK for CPU clock alignment.

CPU Clock Trace Length Calculation for Socket-370 System

Before routing any other signals on the board, pre-route every CPU clock trace from the system clock synthesizer to the Socket-370 CPU (CPUCLK) and North Bridge (HCLK) as short as possible. All high frequency clock alignment will be on the basis of the longest one (usually HCLK). A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → CPU	L_{CPU}	**L_{NB}**	0.5"	1"~9"
Clock chip → VT82C694X (NB)	L_{NB}	**L_{NB}**	-	1"~9"

SDRAM Clock Trace Length Calculation

Pre-route SDRAM clock traces (SDCLK0~SDCLK15) from the system clock synthesizer to the DIMM slots as short as possible. The length of all SDRAM clocks will be based on the longest one (L_{SD}). The length of DCLKWR (L_{DIN}) should be the same as that of the SDCLKs. The DCLKO clock trace should be as short as possible. A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → SDCLK[15:0]	L_{SD}	**L_{SD}**	0.5"	1"~4"
DCLKWR (Clock chip → NB)	L_{DIN} (assume < L_{SD} +3")	**L_{SD} + 4.5"**	0.5"	5.5"~8.5"
DCLKO (NB → Clock chip)	L_{DOUT}	**L_{DOUT}**	-	1"~9"

Note: Here, the 4.5" represents the estimated trace length added into DCLKI for SDRAM clock alignment.

AGP Clock Trace Length Calculation

Pre-route AGP clock traces from the pin GCLKO of the VT82C694X to the AGP slot as short as possible. Then the trace length for the signal GCLK should be the GCLKO trace length plus 3 inches.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
GCLKOUT (NB → AGP Slot)	L_{GOUT}	**L_{GOUT}**	-	1"~9"
GCLKIN (NB → NB)	L_{GIN}	**L_{GOUT} + 3"**	0.5"	4"~12"

Note: Here, the 3" represents the estimated trace length added into GCLKI for AGP clock alignment.

PCI Clock Trace Length Calculation

Pre-route PCI clock traces from the system clock synthesizer to the VT82C694X (NPCLK) and VT82C686A (SPCLK) as short as possible. Then pre-route PCI clock traces PCLK0~PCLK4 from the system clock synthesizer to all PCI slots as short as possible. The length of these clocks will be based on the longest one (L_5). A calculation example is shown below.

Clock Trace	Shortest Length	Desired Length	Allowable Difference	Allowable Range
Clock chip → VT82C694X (NB)	L_{NB}	**L_5 + 3"**	1"	4"~15"
Clock chip → VT82C686A (SB)	L_{SB}	**L_5 + 3"**	1"	4"~15"
Clock chip → PCI1	L_1	**L_5**	1"	1"~12"
Clock chip → PCI2	L_2	**L_5**	1"	1"~12"
Clock chip → PCI3	L_3	**L_5**	1"	1"~12"
Clock chip → PCI4	L_4	**L_5**	1"	1"~12"
Clock chip → PCI5	L_5 (> the others)	**L_5**	-	1"~12"

Note: Here, the 3" represents the estimated trace length added into NPCLK and SPCLK for PCI clock alignment.

Notes for the length calculation of all clock traces:

1. *Shortest length means the minimum routable trace length between both clock ends. Desired length means the real length of the clock traces on PCB layout. Allowable difference means the maximum difference between clock traces of the same type. Allowable range means the acceptable clock length range for the specific clock.*
2. *The location of the system clock chip can affect the length of all clock traces. To optimize the clock alignment, place the clock chip at an appropriate location.*
3. *In addition, the trace impedance of all clock traces should be in the range between 40 ohms and 55 ohms.*

5.4.6 Signal Trace Attribute Checklist

The maximum accumulated trace length as a brief layout reference for high-speed or critical signal groups (e.g. host and memory) is listed in Table 5-4. The accumulated trace length represents the total trace length or the length sum of two traces before and after a damping resistor. It is recommended to route the same signal groups in equal length and as short as possible. A minimum of 5 mils in width and a minimum of 10 mils in spacing are required for all these signals.

Table 5-4. Maximum Accumulated Trace Length

Signal Group	Maximum accumulated trace length	Note
Host Address	4.5”	1
Host Data	4.5”	1
Host Control	4.5”	1
Host Compatibility (from VT82C686A)	As short as possible.	2
Memory Address	4”	
Memory Data	4”	
Memory Control	6”	
AGP Address / Data	6”	3
AGP Strobe	6”	3
AGP Control	6”	3
PCI Address / Data	As short as possible.	4
PCI Control	As short as possible.	4
USB Data	As short as possible.	5
System Management Bus	As short as possible.	6
IDE Data	4.5”	7
IDE Control	4.5”	7

Notes:

1. *When using Socket-370 CPU, VTT termination stub for the host interface should be less than 2”. Both the VTT termination stub and the trace connected to VT82C694X (NB) directly come out the pin of the Socket-370. The location of these termination (56 ohm) resistor networks should be placed as close to Socket-370 CPU as possible. No VTT termination is needed for a Slot-1 CPU based system.*
2. *Each VT82C686A south bridge Open Drain (OD) output control signal to the CPU needs a 150 ~ 450 ohm pull-up which should be placed as close to the VT82C686A chip as possible.*
3. *The trace width of six strobe lines (GDS[1:0], GDS[1:0]#, SBS and SBS#) is 5 mils. Trace length mismatch in any Data/Strobe group should be maintained within 0.5 inch. The maximum pull-up stub trace length on strobe lines and other traces should be less than 0.5 inch. Instead of R-packs, discrete pull-up resistors should be used. It is strongly recommended to keep the stub length as short as possible and maintain the trace length of all AGP (especially Data and Strobe) signals less than 6 inches. It is always best to reduce line mismatch to add to the timing margin. In other words, a balanced topology will match trace lengths within the groups to minimize skew. To minimize signal crosstalk, wider spacing is recommended wherever possible between traces.*
4. *The VT82C694X and VT82C686A should be placed at both ends of the PCI bus for better signal termination.*
5. *Each pair of USB data signals is required to be parallel to each other with the same trace length. Each pair of USB data signals is required to be parallel to a relative ground plane.*
6. *Adding 68pF capacitors to the system management bus at the end device is essential since the I2C bus travels a long way and might pick up noise along the route.*
7. *All signals for primary IDE and Secondary IDE require 33 ohm series termination resistors. These series terminations should be placed as close as possible (less than 1 inch) to the VT82C686A. Data and strobe lines (DD[15..0], IOR#, IOW#, and IORDY#) should be routed as a bus. The total trace length of these signals should be shorter than 4.5 inches. The maximum trace length difference among them must be less than 1 inch. Other lines should be as short as possible. Signal DD7 needs a 10K pull-down on the VT82C686A chip side of the series termination. Signal DREQ needs a 5.6K pull-down on the connector side of the series termination. Signal IRQ14 (and IRQ15) needs a 10K pull-down or pull-up (preferred) on the connector side of the series termination. Signal IORDY# needs a 1K pull-up on the connector side of the series termination. Pin 28 of the IDE connectors should be tied to ground with a 470 ohm serial resistor.*

APPENDICES

The following schematics are provides "as is" with no warranties whatsoever, including any warranty of merchantability, fitness of any particular purpose, or any warranty otherwise arising out of proposal, specification or sample. No license, express or implied, by estoppel or otherwise, to any intellectual property rights are granted herein. VIA Technologies, Inc. disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. VIA Technologies, Inc. does not warrant or represent that such use will not infringe such rights. Third-party brands and names are the property of their respective owners.

Appendix A - Application Circuits of SPKR Strapping

Appendix B - Audio Codec and Game/MIDI Port Layout Guidelines

Appendix C - Apollo Pro133A Reference Design Schematics

Appendix A - SPKR Strapping Application Circuits

Power-up strapping for the VT82C686A SPKR pin (pin V5) determines the function of the Secondary IDE disk data bus pins (SDD[15..0]) to be either SDD[15..0] (SPKR strapped low) or Audio/Game port functions (SPKR strapped high). The speaker drive circuit commonly used in PC motherboards uses a fairly small base resister (on the order of 22 ohms) into the base of a transistor driver. This circuit, however, results in too low a voltage on the SPKR pin for the strap pullup resistor to overcome. In this case, power up reset will always detect a low signal. Therefore, either of the two application circuits shown below in figures A-1 or A-2 should be used to insure that both high and low strap levels are detected properly.

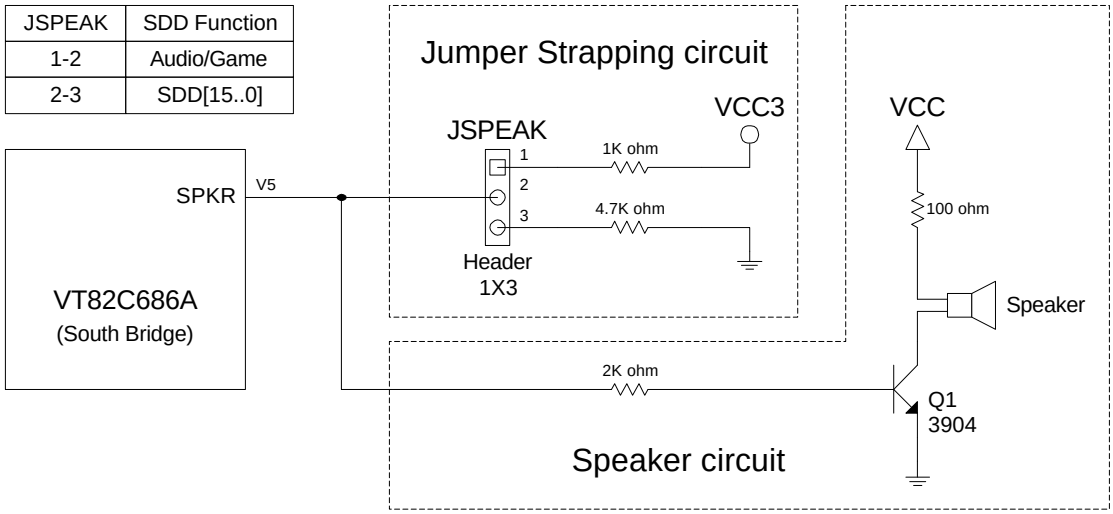


Figure A-1. VT82C686A SPKR Pin Transistor Driver Solution (I)

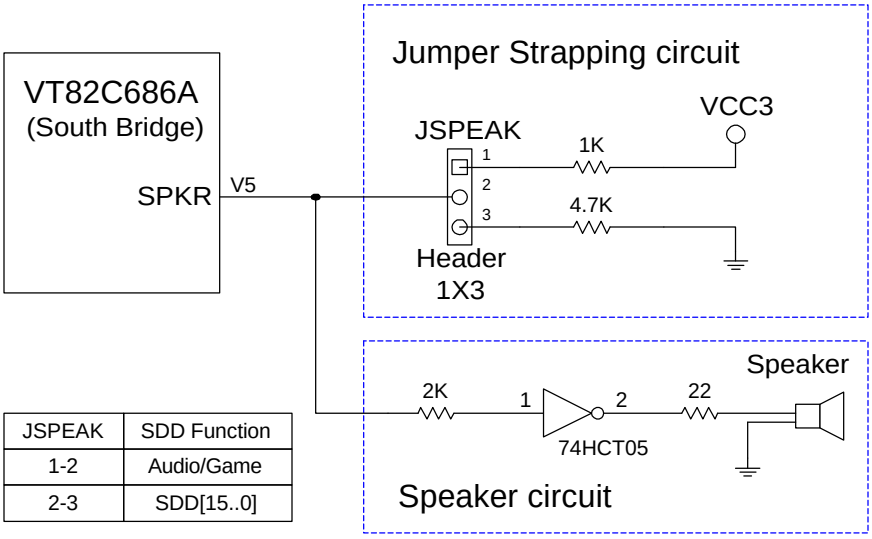


Figure A-2. VT82C686A SPKR Pin Inverter Driver Solution (II)

Appendix B - Audio Codec and Game/MIDI Port Layout Guidelines

B.1 Introduction

This document describes the Printed Circuit Board (PCB) layout recommendations for VIA VT1611A (AC'97 audio codec) and Game/MIDI port in a motherboard design. The main focus is on how to improve the audio quality. Electromagnetic interference (EMI) issues are not considered in the document. The layout guidelines of component placement, power and ground planes and signal routing for VT1611A and Game/MIDI port (using a stacked LINE_OUT, LINE_IN, MIC_IN and Game/MIDI IO connector) on a motherboard are described in detail in the following sections.

VIA VT1611A 18-bit ΣΔ audio codec conforms to the AC'97 2.1 specification with excellent analog performance. Refer to VT1611A datasheet for more detail. Figure B-1 shows a typical single audio codec function block diagram and the direct connections between the VT82C686A south bridge controller and the Game/MIDI port. Audio input/output signals are processed by VT1611A audio codec. Through the AC'97 link, VT1611A audio codec is controlled by VIA VT82C686A south bridge controller.

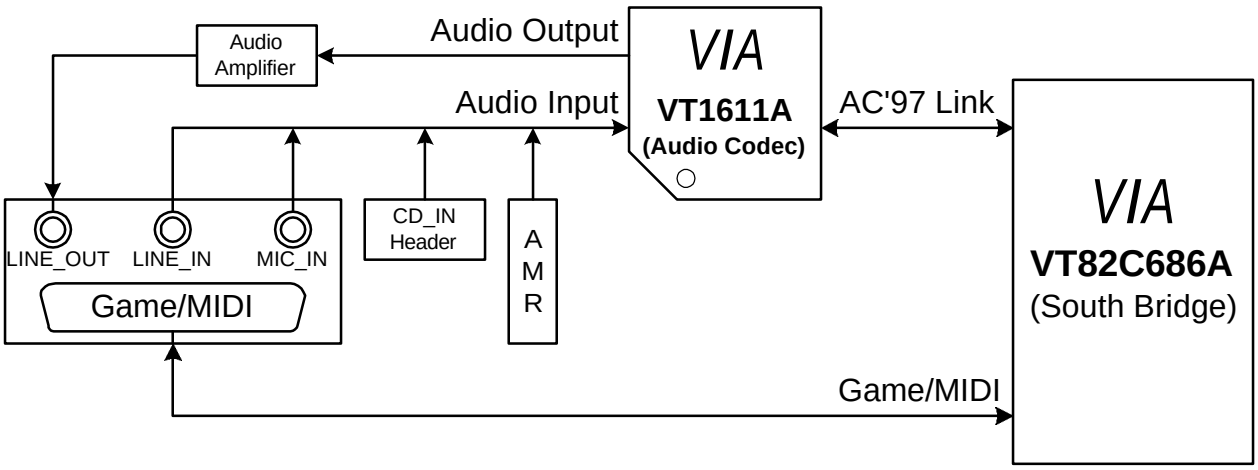


Figure B-1. AC'97 Audio Codec and Game/MIDI Port Block Diagram

Reference AC'97 audio codec and Game/MIDI port schematic is shown in the end page of this appendix. The reference schematic shows an applicable AC'97 audio codec circuit. Five audio input circuits and one audio output circuit are applied. The connections between VT82C686A and the Game/MIDI port are also shown in the schematic.

B.2 Layout Recommendations

In this section, the layout recommendations on component placement, ground and power plane partitions and routing guidelines are described in detail. The PCB layer sequence used here is Signal (Component)-Ground-Power-Signal (Solder).

B.2.1 Component Placement

AC'97 Audio Codec and Audio Amplifier

AC'97 audio codec (VT1611A) and audio amplifier (TPA122) are two major components in the audio codec circuitry. An example placement for AC'97 audio codec and audio amplifier on either ATX or micro-ATX form factor is shown in Figure B-2. To limit the audio analog grounding area (GND_AUD), it is not recommended to place the audio codec far from the LINE_OUT, LINE_IN and MIC_IN audio jacks. And the audio amplifier should be located right beside the LINE_OUT audio jack because the audio line out signals are very sensitive to noise from any other signals.

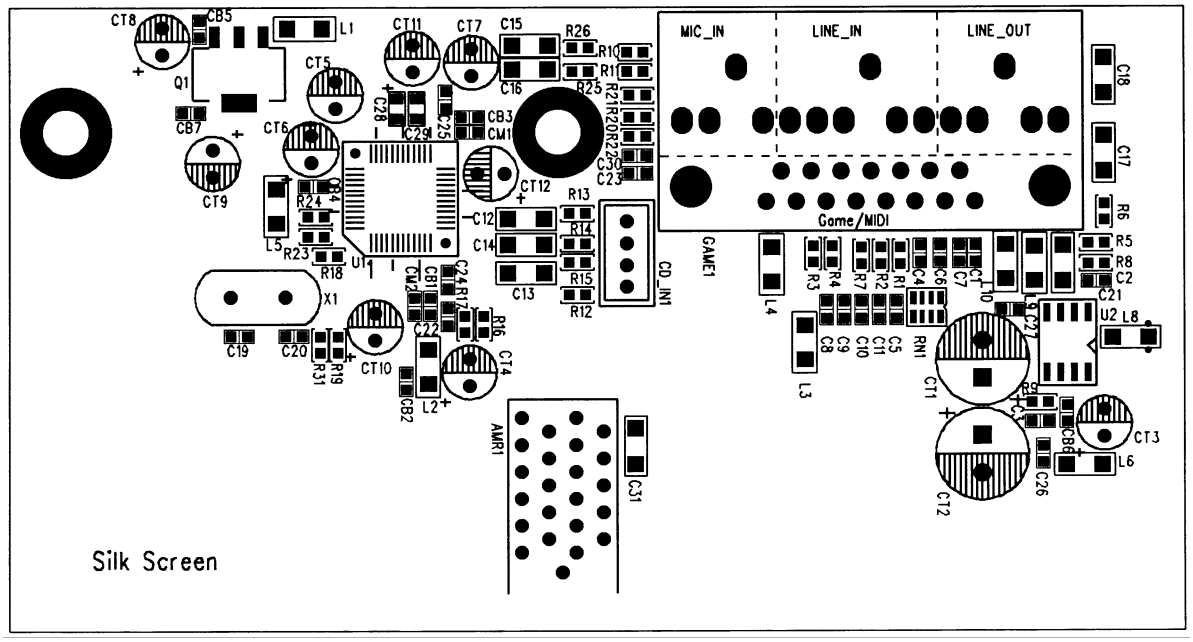


Figure B-2. AC'97 Audio Codec and GAME/MIDI Port Placement Example

VDD/VSS Capacitive Decoupling

There are analog power signals (two pairs of AVDD/AVSS signals) and digital power signals (two pairs of DVDD/DVSS signals) on VT1611A audio codec. Local regulation converting from +12V power for analog power supply to VT1611A is strongly recommended. No local regulation is required for DVDD power supply to VT1611A. Directly using on-board +5V power can already provide adequate digital power supply to VT1611A through a ferrite bead.

All high frequency AVDD5 decoupling capacitors (less than 10uF, ceramic) should be placed very close to the AVDD/AVSS pins of VT1611A and the connection from codec pin to capacitor pad should be routed on the same layer with a short and wide trace (or a small power plane). That is, there should be no vias connecting the decoupling capacitor to the device pin. All high frequency DVDD5 decoulping capacitors should have short wide traces connecting to DVDD/DVSS to decrease ground bounce and other noise coupling caused from digital switching. These high frequency DVDD5 decoupling capacitors should be placed very close to the DVDD/DVSS pins of VT1611A. All high frequency AVDD decoupling capacitors should use the same way described above.

These high frequency decoupling capacitors should be routed on the component layer with wide traces to reduce impedance and placed on their respective ground plane.

Low frequency decoupling capacitors (basically greater than or equal to 10uF, Electrolytic or Tantalum) are used to prevent power supply droop during load transient. These large 10uF low frequency VDD (AVDD or DVDD) decoupling capacitors do not need to be placed close to the codec, but do need to be placed over the proper ground plane. That is, the DVDD decoupling capacitors should be placed over digital ground and the AVDD decoupling capacitors should be placed over analog ground. See ground and power planes section for more information. The low frequency decoupling for the +12V input to the regulator are also over the digital plane.

Referring to Figure B-2, high frequency decoupling capacitors CM1 and CB4 are placed very near the one pair of AVDD and AVSS pins (pins 25 and 26) and the other pair of AVDD and AVSS (pins 38 and 42) respectively. The location of low frequency decoupling capacitors CT5 and CT6 are also close to analog power and ground pins. Similarly, decoupling capacitors CB1, CM2 and CT10 are located very near the digital power and ground (DVDD and DVSS) pins. Decoupling capacitors CB6, and CT3 are located very near the analog power and ground (VAA and GND) pins of audio amplifier.

Table B-1. Decoupling Capacitor List

Power plane	High Frequency Capacitors	Low Frequency Capacitors	Ferrite Bead	Note
AVDD5	CB4, CM1	CT5, CT6	L5, L1	
DVDD5	CB1, CM2	CT10	L2	
AVDD	CB6	CT3	L6	

Voltage Reference Bypass and Filter Capacitors

All high frequency decoupling capacitors for the voltage reference should be placed close to the VT1611A chip and routed on the component layer with wide traces to reduce impedance. The filter capacitors on the VREF, VREFOUT, AFILT1 and AFILT2 pins should also be top routed and laid close to the codec pins.

Referring to Figure B-2, high frequency decoupling capacitors CB3, C25, C28 and C29 are placed very near the pins VREF, VREFOUT, AFILT1 and AFILT2 (pins 27, 28, 29 and 30 respectively).

AC-Coupling Capacitors

It is recommended to place all ac-coupling capacitors as close to the device receiving the signal as possible even though they are not critical. Table B-2 and Table B-3 respectively list the ac-coupling capacitors for audio input and output signals in the example schematics. When an audio function is not used, the ac-coupling capacitors for it are no longer needed. That is, take away the ac-coupling capacitors and leave the pins open, such as MIC_IN_2.

Table B-2. AC-Coupling Capacitors for Audio Input Signals

Audio Input Signals	AC-Coupling Capacitors	Note
CD_L	C13	1
CD_R	C12	1
CD_GND	C14	1
LINE_IN_L	C15	1
LINE_IN_R	C16	1
PC_BEEP	C24	1
MIC_IN_1	C23	1
MIC_IN_2	*None*	1,2
AUX_IN_L	*None*	1,2
AUX_IN_R	*None*	1,2
VIDEO_L	*None*	1,2
VIDEO_R	*None*	1,2

Table B-3. AC-Coupling Capacitors for Audio Input Signals

Audio Output Signals	AC-Coupling Capacitors	Note
LINE_OUT_L	C17	1
LINE_OUT_R	C18	1
MONO_OUT	*None*	1,2
LNLVL_OUT_L	*None*	1,2
LNLVL_OUT_R	*None*	1,2

Notes
1. Use all ac-coupling capacitors in 1206 package.
2. Use the same ac-coupling mechanism when the function is applied.

These audio input ac-coupling capacitors in Table B-2 should be placed near the audio codec. For example, C13, C12, and C14 should be placed near pins CD_L, CD_R and CD_GND of the audio codec respectively since they take their CD-in signal from the CD_IN header.

The line-out signals are delivered from the audio codec to the LINE_OUT jack through the audio amplifier. Therefore, these audio output ac-coupling capacitors in Table B-3 should be placed near the audio amplifier. C17 and C18 should be placed near pins INB and INA of the audio amplifier respectively since they receive the line-out signal from the audio codec. This audio amplifier should be placed close to the LINE_OUT jack from preventing any noise coupling.

Referring to Figure B-2, C15, C16 and C23 are close to the audio codec since they take their signal from the LINE_IN and MIC_IN jacks. The ac-coupling capacitors C13, C12 and C14 are close to the audio codec since they take their signal from the on-board CD_IN header. The ac-coupling capacitor C24 is close to the audio codec since it receives the speaker signal from the VT82C686A south bridge controller.

Voltage Regulators

The DC-DC voltage regulator supplies the 5V analog power to the audio codec from +12V system power. In this manner, noise form other digital powers can be isolated by the regular and a quiet analog power can be obtained through a ferrite bead. The +12V input and 5V output (VDD5) routings should be made over the digital ground plane. The 5V output is set close the analog section of the codec through a ferrite bead. The analog 5V routing (AVDD5) should be over the analog ground plane. See Section B.2.2 for more information on digital and analog ground planes.

Referring to Figure B-2, the regulator locating on the upper-left side of the audio codec can provide the shortest power path to the audio codec.

On-board Audio Connectors

CD_IN headers and other on-board audio connectors such as telephony audio can be placed anywhere over the analog ground plane. That is, they do not need to be close to the codec, but do need to be enclosed by a ground plane. The analog ground plane is chosen since it is the quietest ground.

Referring to Figure B-2, the CD_IN header was placed close to the codec and the ac-coupling capacitors C12, C13 and C14 as well as resistors R12, R13, R14, and R15 were laid between the codec and header to keep the layout tight to reduce noise coupling and DC offsets.

B.2.2 Ground and Power Planes:

It is recommended to include partitioned digital and analog power planes directly over their respective ground planes. The power-ground sandwich with a substrate separation can provide an extremely effective, low ESR & ESL bypass capacitance. The audio IC leads will have pads and vias that go directly to the appropriate plane for power and ground. All digital components are mounted over the digital power/ground plane sandwich and all analog components over the analog power/ground sandwich. This doesn't avoid the need for additional ceramic bypass capacitors at the IC pins as mentioned above. The importance and effectiveness of ground planes cannot be over emphasized to optimize the performance of the codec.

Ground planes

VIA recommends having separate analog and digital ground planes on the PCB ground layer (2nd layer in our case). All digital pins of the codec and all digital support components should be over the digital ground. All analog pins and analog support components should be over the analog ground plane. Three analog ground planes (GND_AUD, GND_LOUT and GND_MIDI) and one digital ground plane (GND) are shown in Figure B-3. Table B-4 lists the audio signals covered by different ground planes. The line out circuit should refer to its own analog ground partition (GND_LOUT) instead of GND_AUD for better signal consideration.

All digital routing should not run over the analog plane. If it is necessary to route a digital signal over the analog plane the trace length should be short and the digital signal should be static. All analog routing should be over the analog plane. When analog signals need to cross the gap in the ground plane (when connecting the jacks for example) components such as ferrite beads or 0 ohm shorts should be used. Signal traces should never cross the gap between the ground planes.

The analog ground and digital ground planes should be connected through only one ferrite bead (preferred) or a series 0 ohm resistor. The recommended location for the ferrite bead or the 0-ohm resistor is on the quietest area where have no signals passing around.

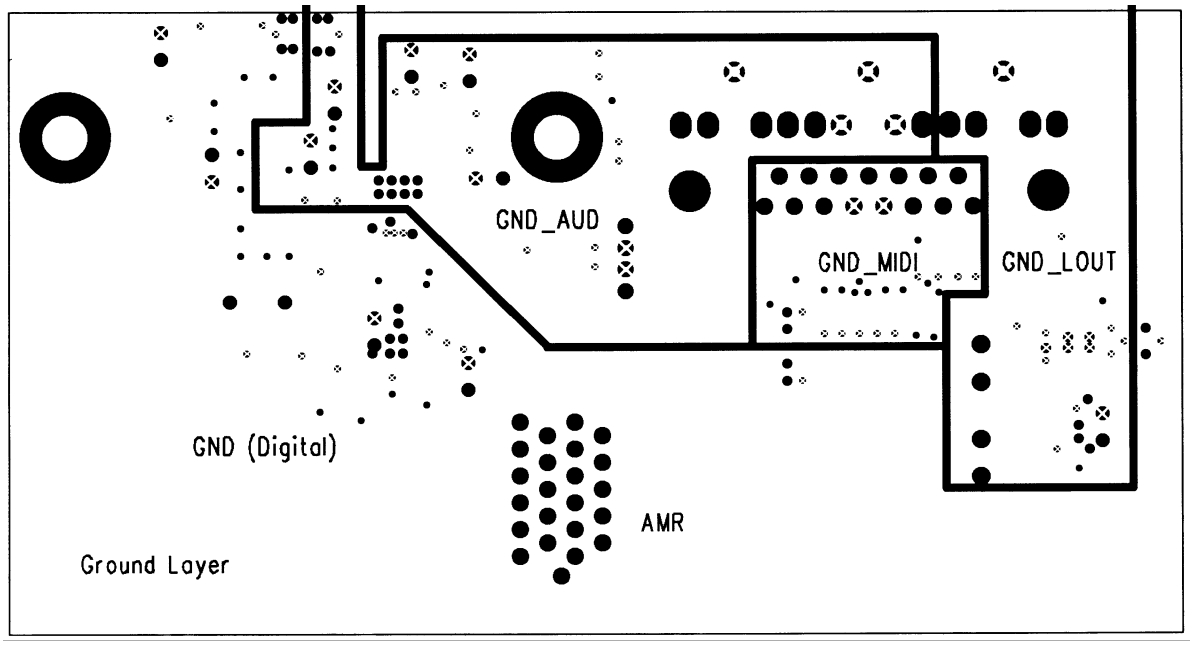


Figure B-3. Ground Layer Layout Example

Table B-4. Signal Groups Associated with Their Audio Ground Plane

Ground Planes	Audio Signals	Note
GND_AUD	**Audio input signals**: AUX_L. AUX_R, VIDEO_L, VIDEO_L, VIDEO_R, CD_L. CD_R, CD_GND, LINE_IN_L, LINE_IN_OUT, MIC1, MIC2, PHONE_IN **Audio reference signals**: MONO_OUT, VREFOUT, VREF, AFILT1 and AFILT2 **Analog Power signals**: AVDD1, AVDD2, AVSS1 and AVSS2	
GND_LOUT	**Audio output signals**: LINE_OUT_L, LINE_OUT_R, LNLVL_OUT_L and LNLVL_OUT_R	
GND_MIDI	**Game/MIDI port signals**: JAB1, JBB1, JACX, JACB, MSO, JBCY, JACY, JBB2, JAB2	
Digital Ground	**Digital power signals**: DVDD1, DVDD2, DVSS1 and DVSS2 **AC link signals**: SYNC, SDIN, SDOUT, -ACRST, and BIT_CLK **Miscellaneous signals**: XTL_IN, XTL_OUT, PC_BEEP, EAPD, ID1 and ID0	

Power planes

Referring to Figure B-4, no analog power plane partitions on the PCB power layer (3rd layer in our case) is required since all audio signals had been laid on the component layer. These signals can directly refer to their respective ground plane. The power planes represented on the component or solder layer should be placed directly over their respective ground plane. For example, the AVDD5 power plane should not be outside of the GND_AUD (analog ground) plane.

All analog power supply connections and routing on the component layer should be over the analog ground planes and all of the digital power connections and routing on the component layer should be over digital ground planes. The +12V input voltage to the regulator should be a wide trace that routes over the digital ground plane. +12V routing over digital planes and located near the edge of the board. Analog section is well bounded making it easy to create power/ground sandwich.

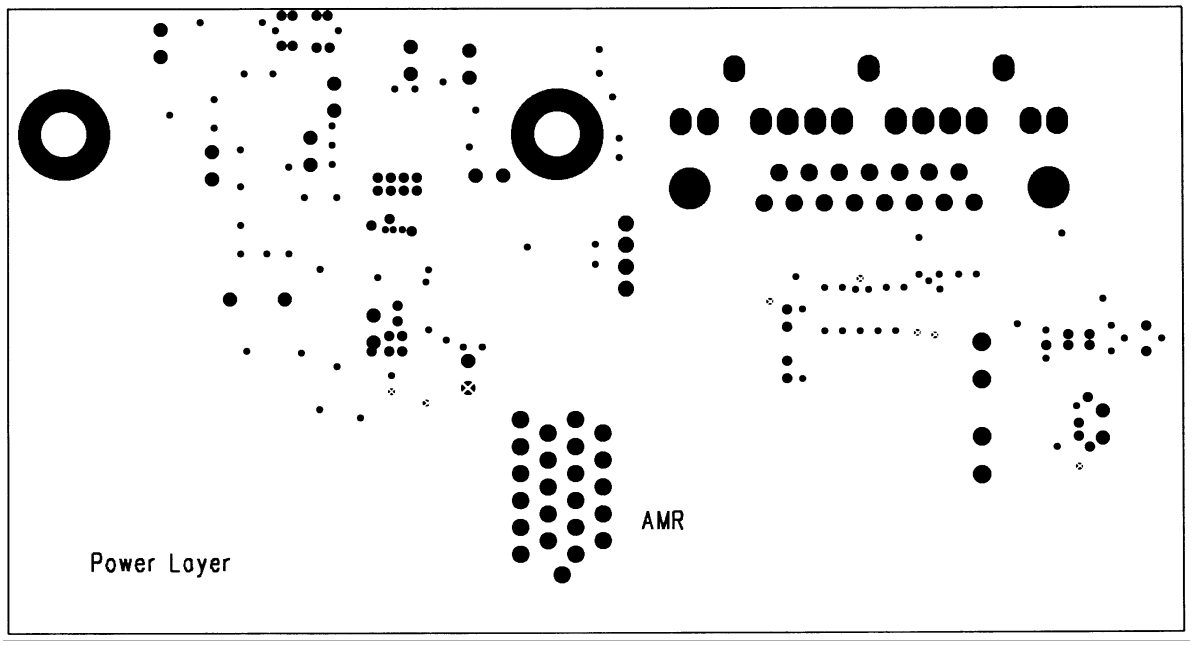


Figure B-4. Power Layer Layout Example

B.2.3 Routing Guidelines

Routing to VDD, VREF, AFILT and FILT capacitors

All high frequency decoupling, reference high frequency decoupling and filter capacitors must be routed on the same layer as the codec. This is done to reduce inductance in the supply, reference and filter networks. Inductive loops in these networks can be a coupling mechanism for high frequency noise. High frequency noise can then be aliased down into the audio band during the A/D or D/A process.

Audio Input/Output Routing

Keeping traces short can decrease inductance and help avoiding magnetic coupling. This allows a straight-line route and also allows for shielding with ground traces. Regions between analog signal traces should be filled with copper; the copper fill should be shorted to the analog ground plane. This will help to reduce high frequency interference by creating a capacitance coupling mechanism from signal to ground.

AC'97 Link Routing

The AC'97 link signals should be as short as possible. If the signal traces need to be long certain pre-cautions should be made to reduce ringing and signal reflections. Clock signal such as BIT_CLK should have a series resistor close to the codec. Other clocks like the 24.576MHz clock should have series resistor by the clock source. If a 24.576MHz crystal is used series resistance is not required. This series resistance in the clock lines will help to reduce reflections. A shunt capacitor should also be used on these clock lines to help reduce ringing. Preferably the capacitors should be placed close to the clock source but should be electrically connected to the opposite side of the series resistor. It is also recommended to place series resistors on the SDATA_IN and SDATA_OUT lines. The resistors should be placed close to the signal source.

The use of ground trace shields may also help to reduce noise coupling and radiation from the digital link. Therefore, regions between digital signal traces should be filled with copper. The copper fill should be shorted to the digital ground plane. Therefore, excellent shielding through capacitive coupling can be achieved.

Referring to Figure B-5, the AC'97 link signals should come in from the lower side of the audio codec to keep them far from the analog signals.

Game/MID Signals Routing

The Game/MIDI resistor-capacitor components should be placed on the analog Game/MIDI ground (GND_MIDI) and as close to the Game/MIDI port as possible.

Referring to Figure B-6, the Game/MIDI signals should come in from the lower side of the Game/MIDI port to keep them far from other analog signals.

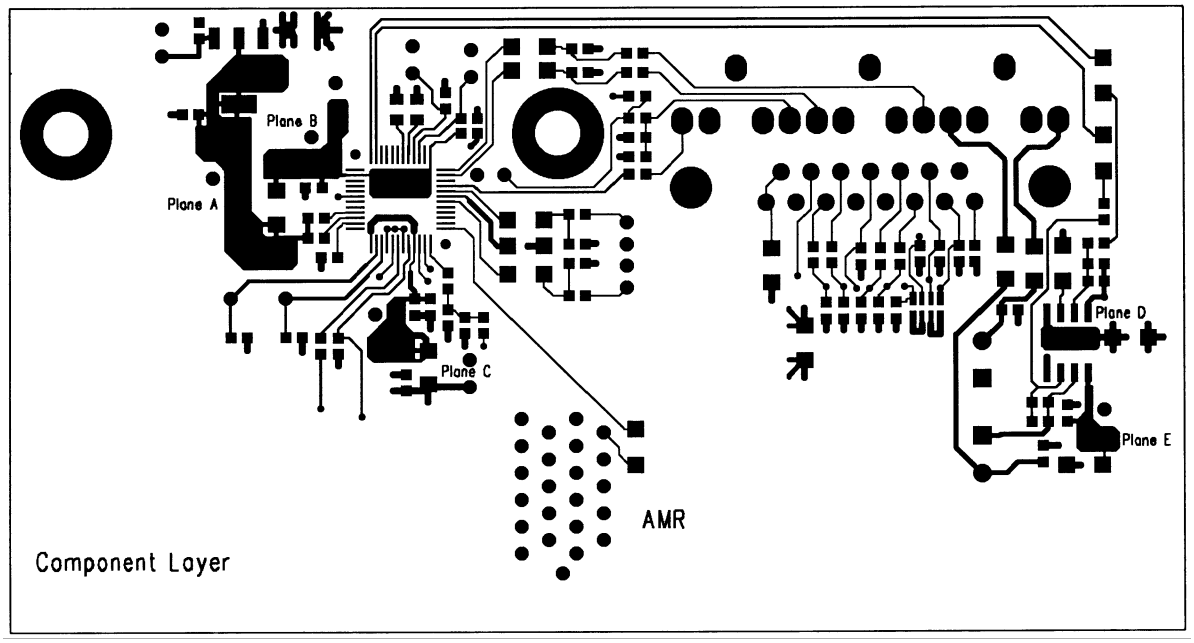


Figure B-5. Component Layer Layout Example

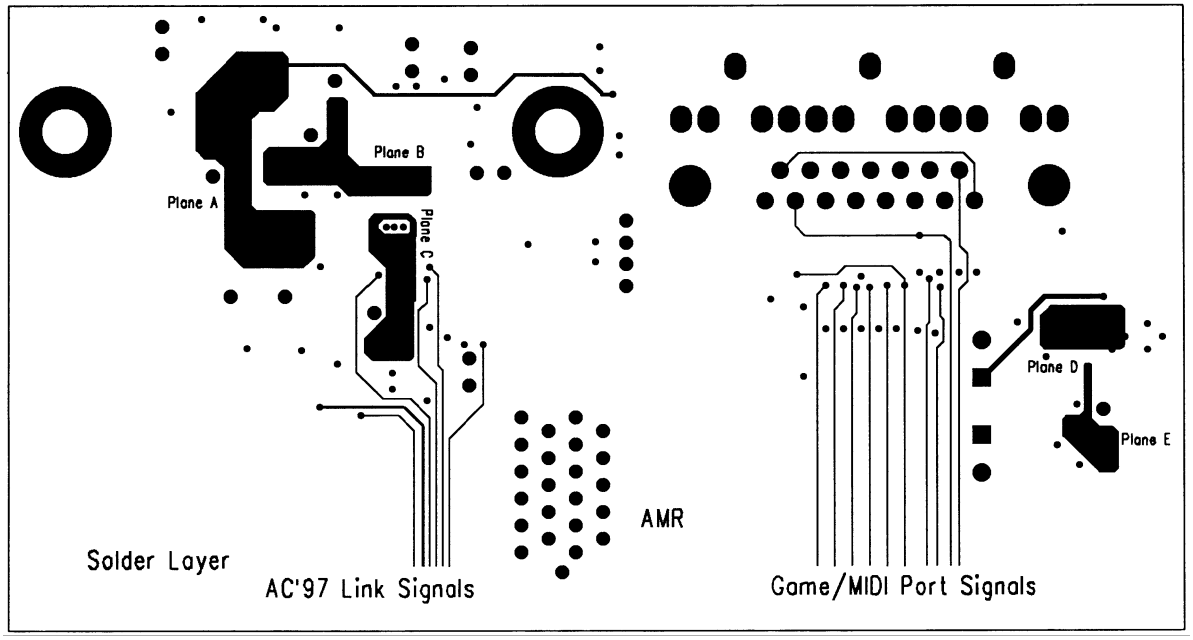


Figure B-6. Solder Layer Layout Example

Table B-5 and Table B-6 show the layout guideline summary for signal and power/ground nets respectively in the reference schematic.

Table B-5. Routing Guidelines for Signal Nets

Net Name	Routing Guidelines	Note
SYNC, SDIN, SDOUT, -ACRST	Maintain 8 mil trace width and 12 mil spacing	1
BITCLK	Maintain at least 10 mil trace width and 20 mil spacing	1
PC_BEEP, ID1, ID0, EAPD	Maintain 8 mil trace width and 12 mil spacing	1
XTLI, XTIO	Maintain 15 mil trace width and 20 mil spacing	1
CDL, CDR	Maintain 8 mil trace width and 12 mil spacing	1
CDGND	Maintain 20 mil trace width and 20 mil spacing	1
MICIN	Maintain 10 mil trace width and 20 mil spacing	1
LINE_L, LINE_R	Maintain 8 mil trace width and 12 mil spacing	1
AFILT1, AFILT2, VREF, VREFOUT	Maintain 10 mil trace width and 20 mil spacing	1
LINEOUTL, LINEOUTR	Maintain 10 mil trace width and 20 mil spacing all the way through audio amplifier to LINE_OUT jack.	1

Note: Wherever possible, keep the spacing as wide as possible for all signals.

Table B-6. Routing Guidelines for Power and Ground Nets

Net Name	Routing Guidelines	Note
AVCC5	Maintain small power island (plane) or short and wide (as wide as possible) trace to ferrite bead L5 before providing power to AVDD5	1
AVDD5	Maintain small power island (plane) or short and wide (as wide as possible) trace to pins AVDD1 and AVDD2 of VT1611A	1
DVDD5	Maintain small power island (plane) or short and wide (as wide as possible) trace to pins DVDD1 and DVDD2 of VT1611A	1
AVDD	Maintain small power island (plane) or short and wide (as wide as possible) trace to pin VAA of TPA122 audio amplifier	1
GND_AUD, GND_LOUT, GND_MIDI	Maintain 20 mil trace width on the component layer through a ferrite bead and then multiple vias to digital ground	2

Notes:

1. *Refer to power planes A, B, C and D in Figure B-5 and Figure B-6 for AVCC5, AVDD5, DVDD5 and AVDD respectively.*
2. *Refer to analog ground planes in Figure 3 for GND_AUD, GND_LOUT and GND_MIDI and ground plane E for GND_LOUT in Figure B-5 and Figure B-6.*

Appendix C - Apollo Pro133A Reference Design Schematics

Apollo Pro133A Reference design schematics are shown in the following 20 pages. The component placement for this reference design is shown in Figure C-1. The system specification for this motherboard design is listed below:

- ATX Form Factor
- Single Slot-1 CPU (66-133 MHz)
- Apollo Pro133A single chip clock synthesizer
- VT82C694X Apollo Pro133A North Bridge (CPU/AGP/PCI bridge with integrated DRAM controller)
- VT82C686A South Bridge (PCI-to-ISA bridge with integrated I/O controllers)
- Three DIMM Slots (maximum 1.5GB and 133 MHz memory frequency)
- One AGP Slot (66MHz)
- Two PCI Slots (33MHz)
- One ISA Slot (8/16MHz)
- One AMR slot
- Two Enhanced IDE (up to 66MHz) Interfaces
- Four USB (48MHz) Ports
- PS2 Keyboard/Mouse Support
- Ring In, Modem Wake up and LAN Wake up circuitry
- One AC'97 Link Controller (to cooperate with a AC'97 Codec chip)
- One Floppy Drive Interface
- One Infrared Interface
- Various Hardware Monitoring (support 5 positive voltage, 3 temperature, and 2 fan-speed monitoring)
- One parallel Port and Two Serial Ports
- One MIDI/GAME Port
- One 2MB Flash ROM

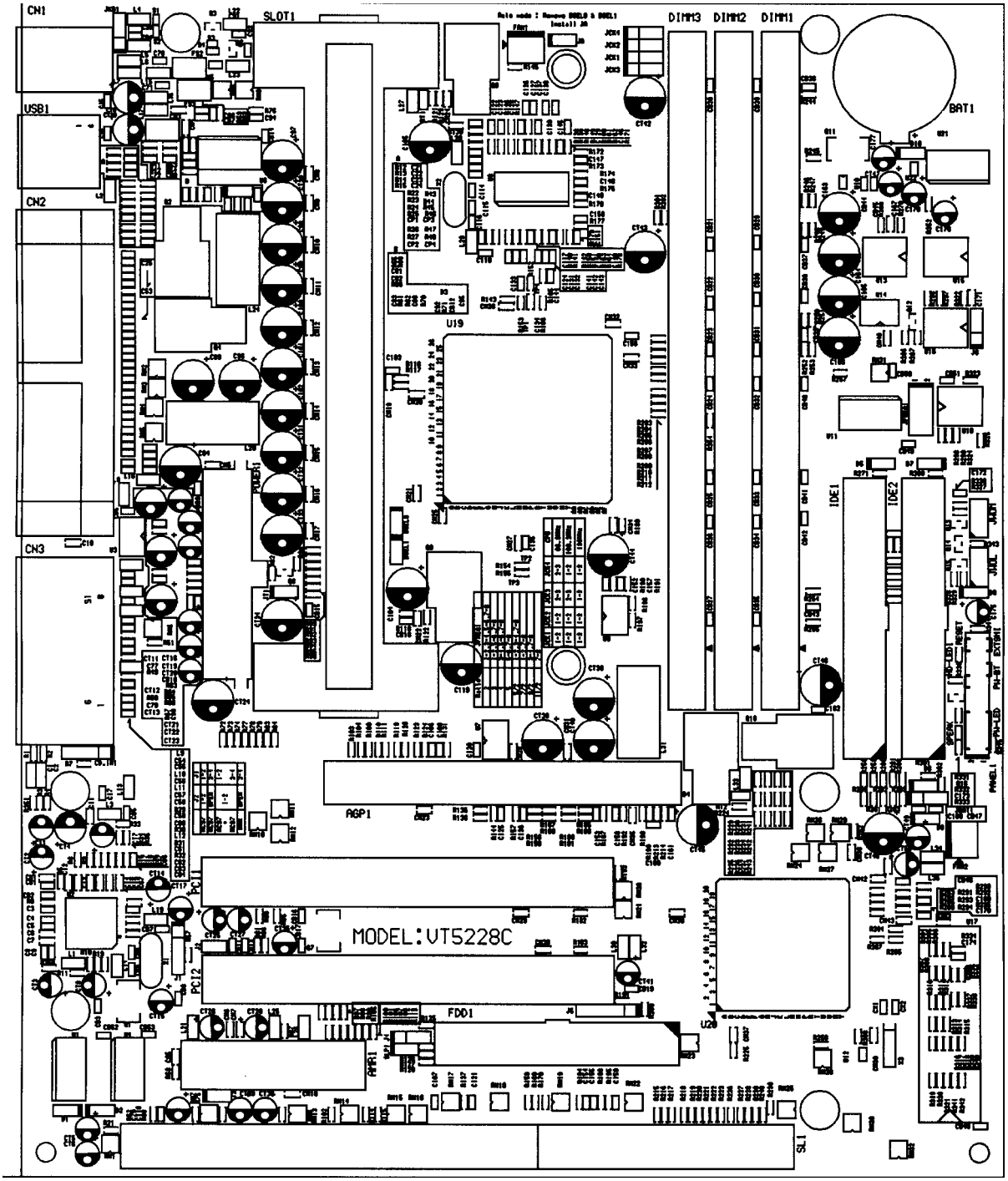


Figure C-1. Apollo Pro133A Reference Component Placement

VIA Preliminary Customer Reference Schematics

MODEL:VT5228C

VER:0.1

(SLOT 1+VT82C694A/X+VT82C686A+AGP2X/4X MODE+STR FUNCTION)

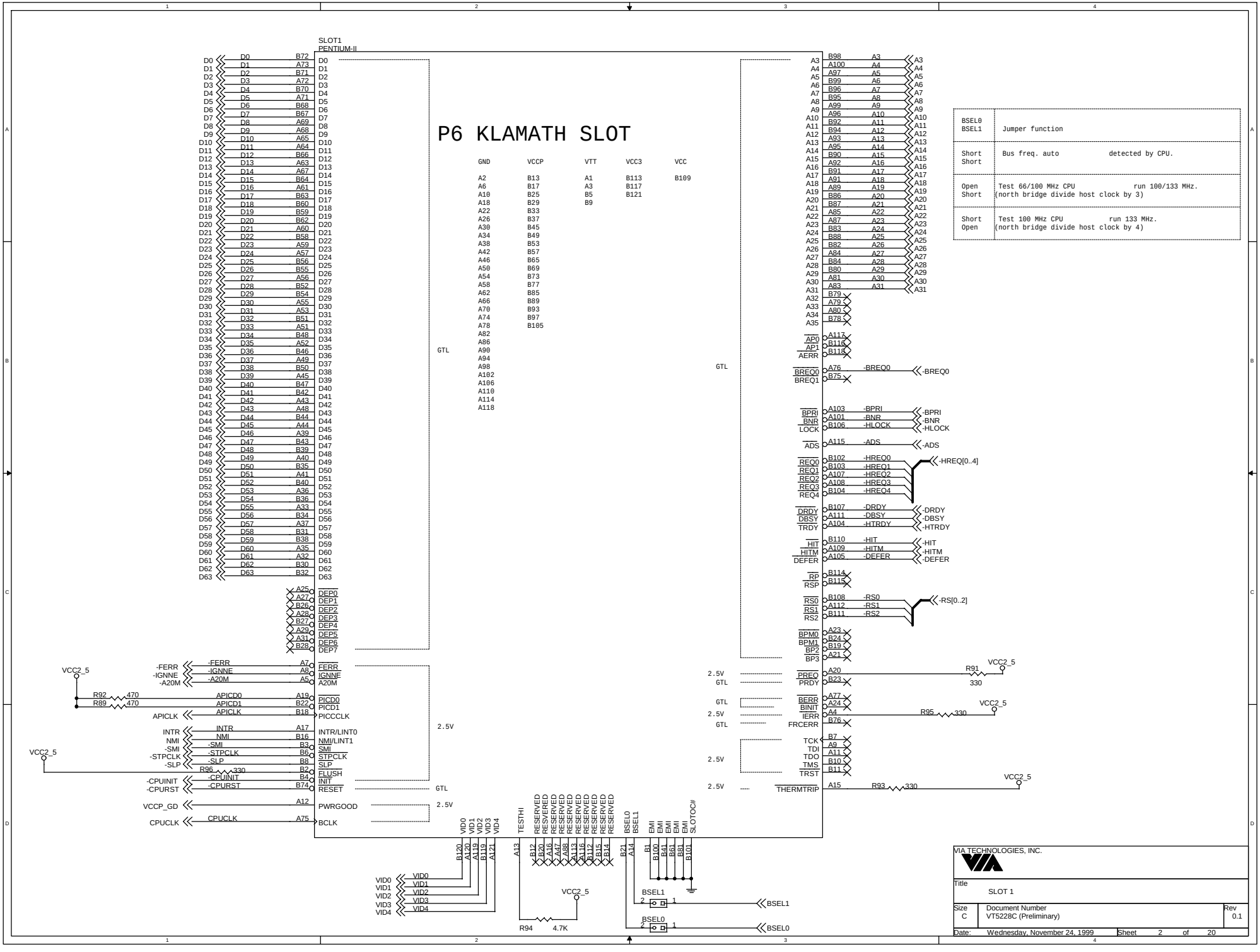
LINK
2.SCH
3.SCH
4.SCH
5.SCH
6.SCH
7.SCH
8.SCH
9.SCH
10.SCH
11.SCH
12.SCH
13.SCH
14.SCH
15.SCH
16.SCH
17.SCH
18.SCH
19.SCH
20.SCH

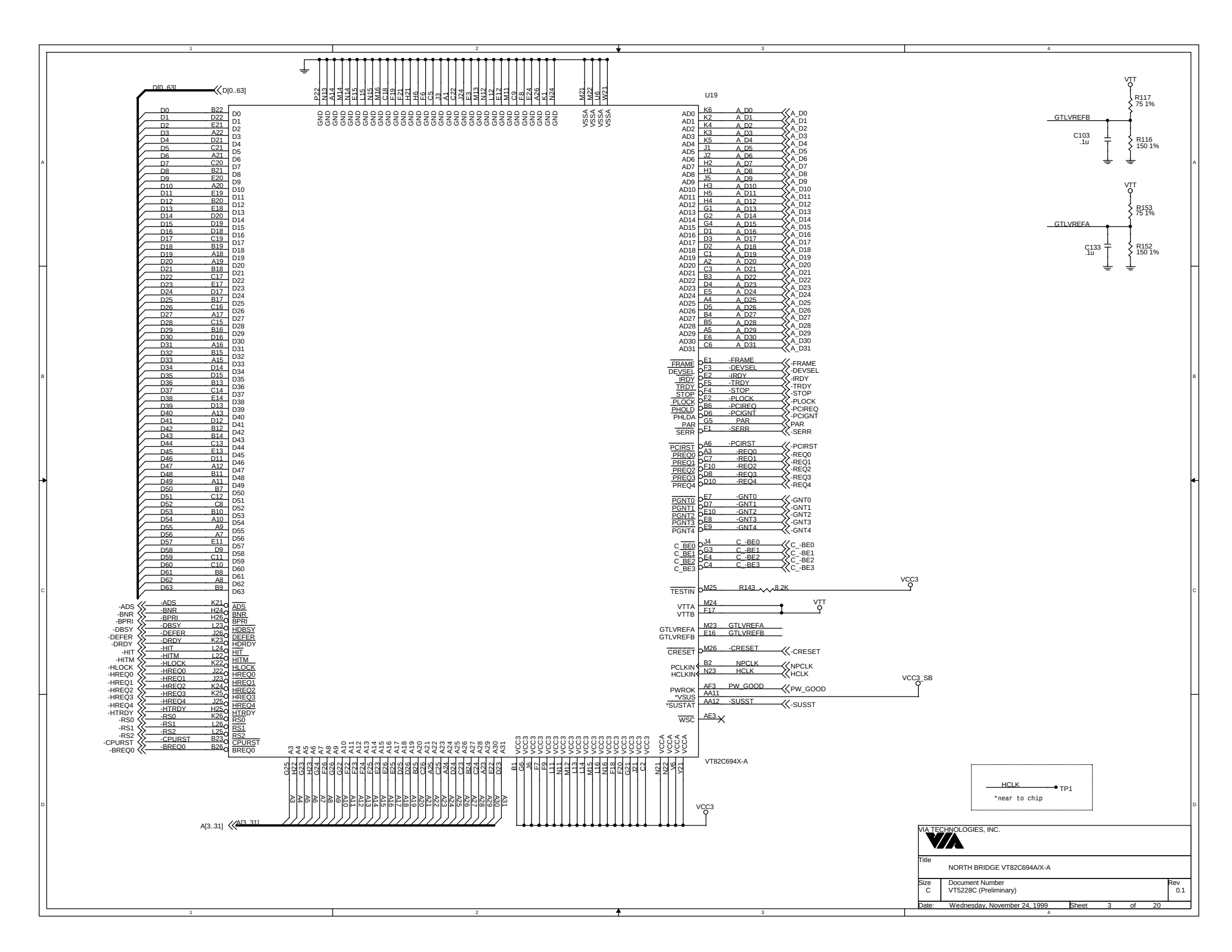
VIA TECHNOLOGIES, INC.

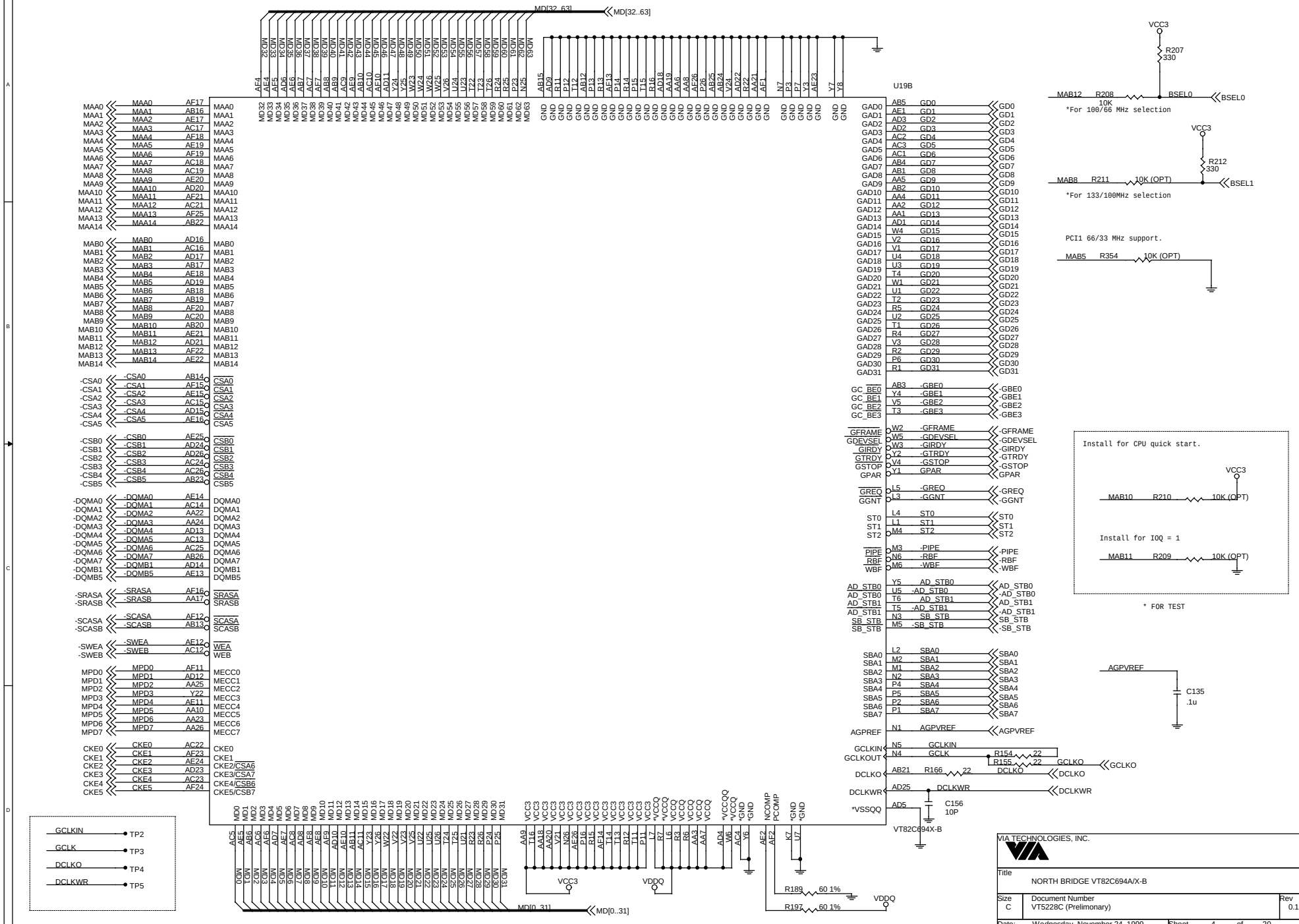
Title: COVER SHEET

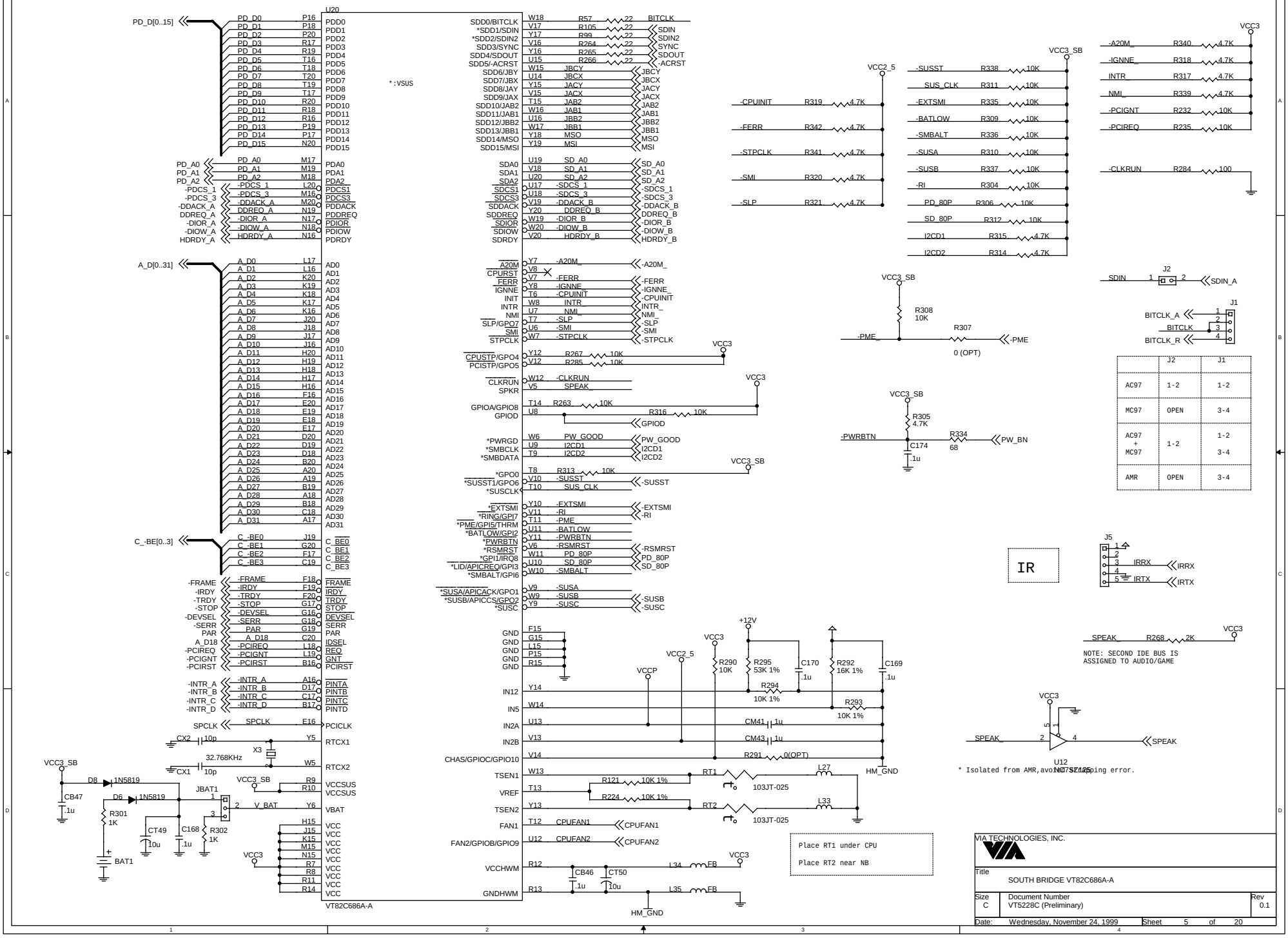
Size: C | Document Number: VT5228C (Preliminary) | Rev: 0.1

Date: Wednesday, November 24, 1999 | Sheet 1 of 20

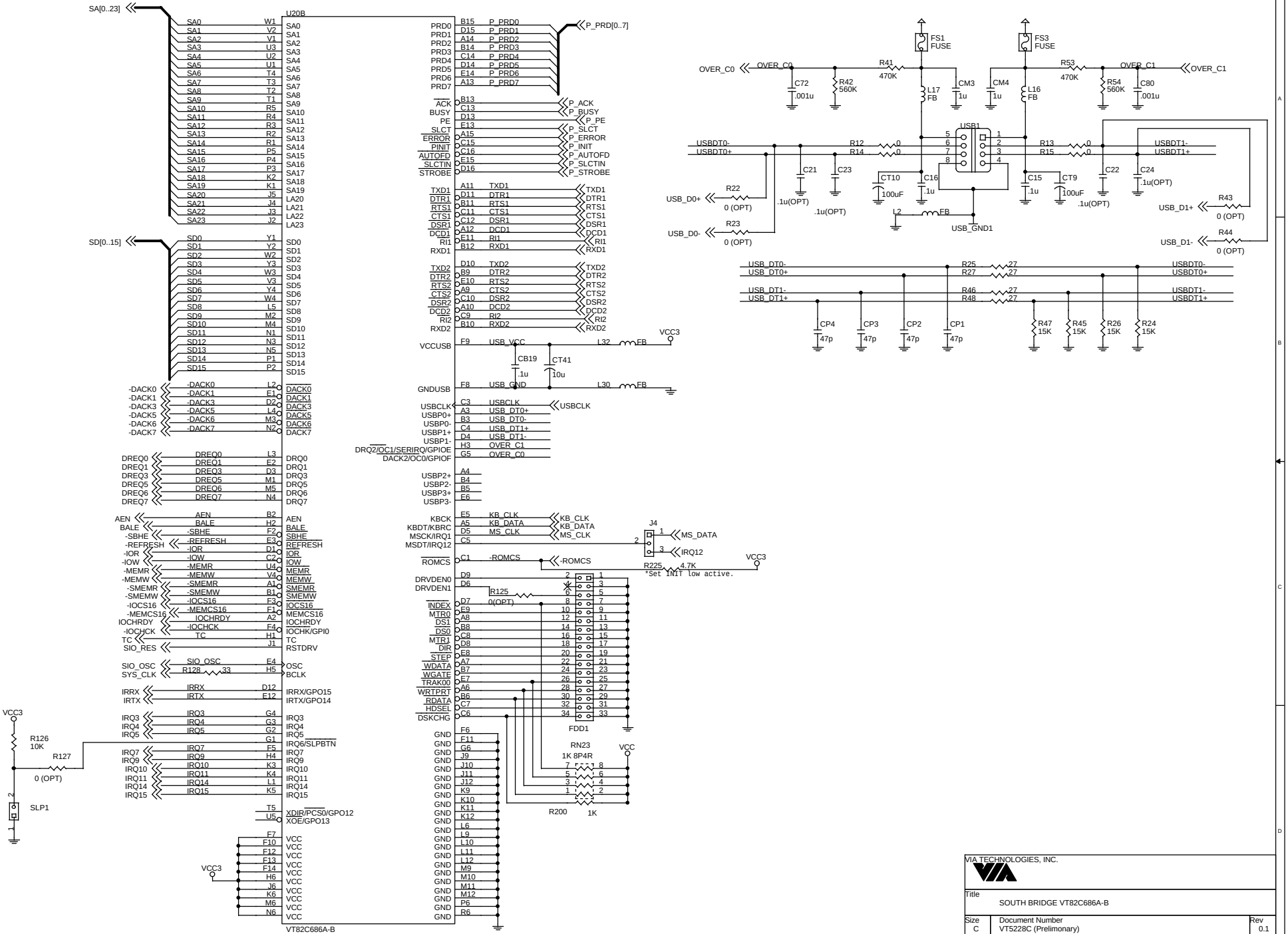

SLOT1
PENTIUM-II
P6 KLAMATH SLOT
GND VCCP VTT VCC3 VCC
A2 B13 A1 B113 B109
A6 B17 A3 B117
A10 B25 B5 B121
A18 B29 B9
A22 B33
A26 B37
A30 B45
A34 B49
A38 B53
A42 B57
A46 B65
A50 B69
A54 B73
A58 B77
A62 B85
A66 B89
A70 B93
A74 B97
A78 B105
A82
A86
A90
A94
A98
A102
A106
A110
A114
A118
GTL
2.5V
BSEL0 BSEL1 Jumper function
Short Short Bus freq. auto detected by CPU.
Open Short Test 66/100 MHz CPU run 100/133 MHz. (north bridge divide host clock by 3)
Short Open Test 100 MHz CPU run 133 MHz. (north bridge divide host clock by 4)
VIA TECHNOLOGIES, INC.
Title
SLOT 1
Size C
Document Number VT5228C (Preliminary)
Rev 0.1
Date: Wednesday, November 24, 1999
Sheet 2 of 20

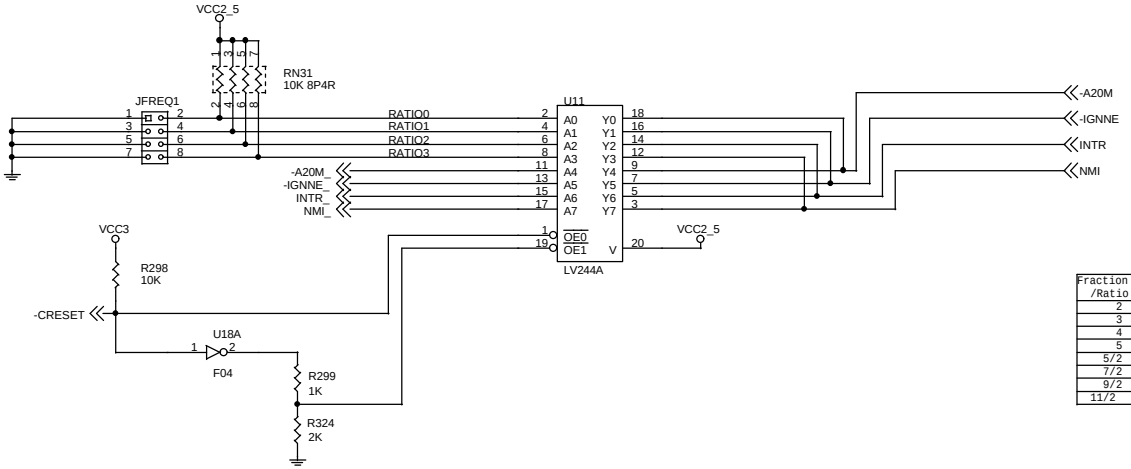

D[0..63]
U19
VT82C694X-A
A[3..31]
VCC3
VCC3_SB
VTT
GTLVREFB
GTLVREFA
R117 75 1%
R116 150 1%
R153 75 1%
R152 150 1%
C103 .1u
C133 .1u
R143 8.2K
HCLK
TP1
*near to chip
VIA TECHNOLOGIES, INC.
NORTH BRIDGE VT82C694A/X-A
Document Number VT5228C (Preliminary)
Rev 0.1
Date: Wednesday, November 24, 1999
Sheet 3 of 20


MD[32..63]
MD[0..31]
U19B
VT82C694X-B
VCC3
VDDQ
GCLKIN
GCLK
DCLKO
DCLKWR
TP2
TP3
TP4
TP5
R207 330
R208 10K
BSEL0
*For 100/66 MHz selection
R212 330
R211 10K (OPT)
BSEL1
*For 133/100MHz selection
PCI1 66/33 MHz support.
R354 10K (OPT)
Install for CPU quick start.
R210 10K (OPT)
Install for IOQ = 1
R209 10K (OPT)
* FOR TEST
AGPVREF
C135 .1u
R154 22
R155 22
R166 22
C156 10P
R189 60 1%
R197 60 1%
VIA TECHNOLOGIES, INC.
Title
NORTH BRIDGE VT82C694A/X-B
Size C
Document Number VT5228C (Preliminary)
Rev 0.1
Date: Wednesday, November 24, 1999
Sheet 4 of 20

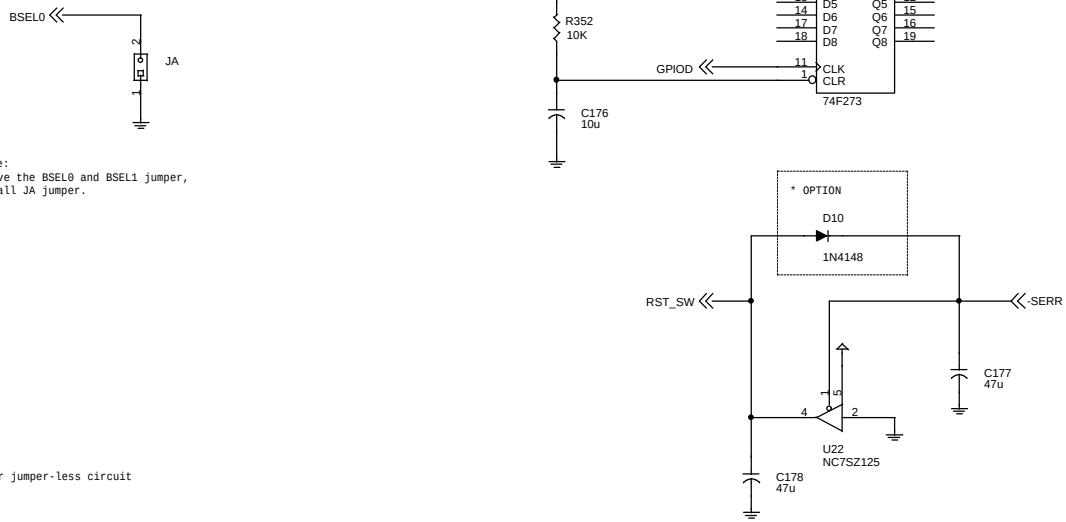


	J2	J1
AC97	1-2	1-2
MC97	OPEN	3-4
AC97 + MC97	1-2	1-2 3-4
AMR	OPEN	3-4


U20B
VT82C686A-B
SA[0..23]
SD[0..15]
P_PRD[0..7]
USB1
FS1
FUSE
FS3
FUSE
J4
MS_DATA
IRQ12
*Set 1MIT low active.
FDD1
RN23
1K 8P4R
SLP1
VIA TECHNOLOGIES, INC.
SOUTH BRIDGE VT82C686A-B
Document Number
VT5228C (Prelimonary)
Rev
0.1
Wednesday, November 24, 1999
Sheet 6 of 20



Fraction /Ratio	JFREQ1
2	1-2,3-4,5-6,7-8
3	1-2,5-6,7-8
4	3-4,5-6,7-8
5	5-6,7-8
5/2	1-2,3-4,7-8
7/2	1-2,7-8
9/2	3-4,7-8
11/2	7-8

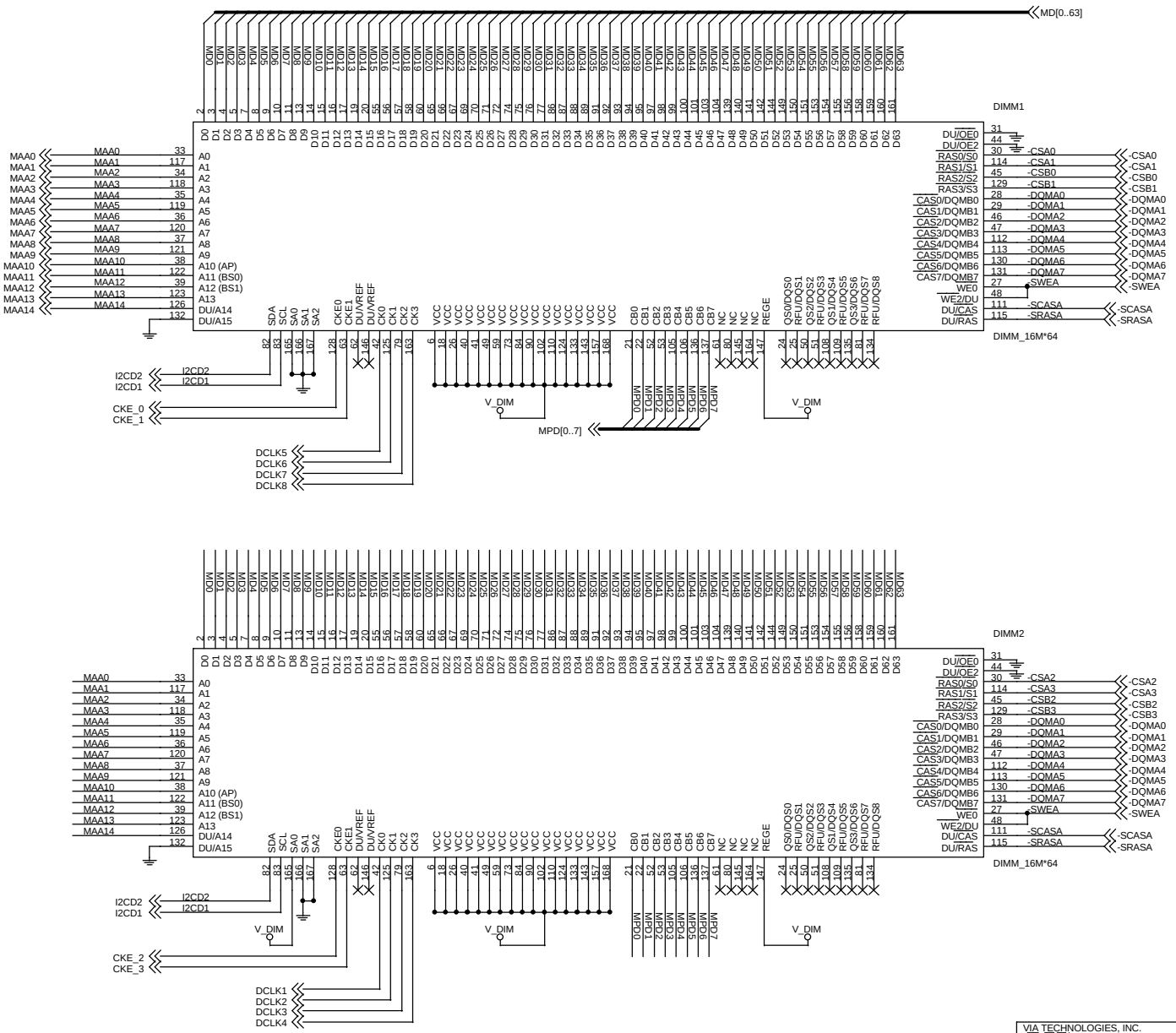


VIA TECHNOLOGIES, INC.

Title: USB2,3 / FREQ. RATIO

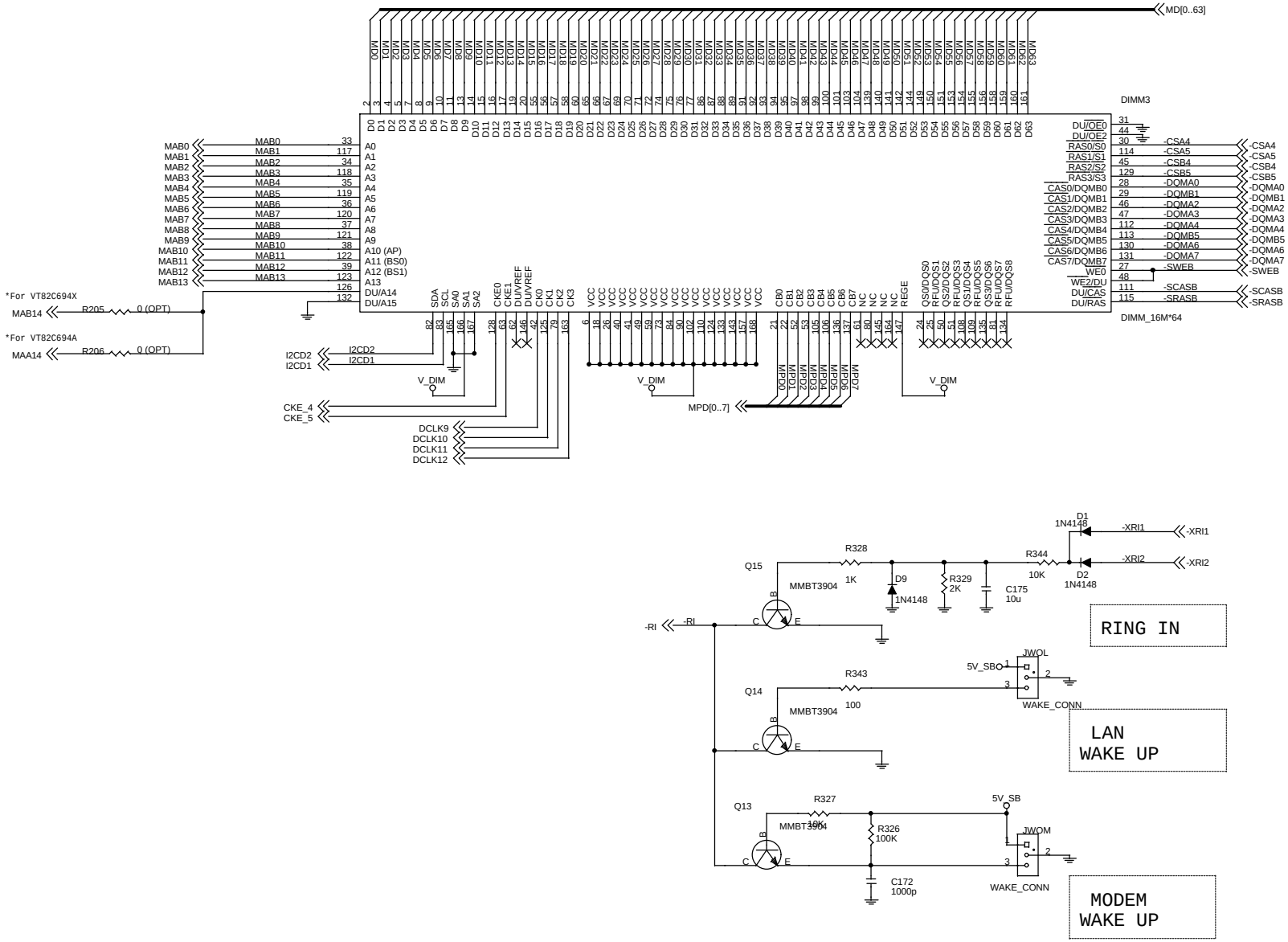
Size	Document Number	Rev
C	VT5228C (Preliminary)	0.1

Date: Wednesday, November 24, 1999 Sheet 7 of 20



VIA TECHNOLOGIES, INC.

Title: SDRAM		
Size: C	Document Number: VT5228C (Preliminary)	Rev: 0.1
Date: Wednesday, November 24, 1999	Sheet 8 of 20	

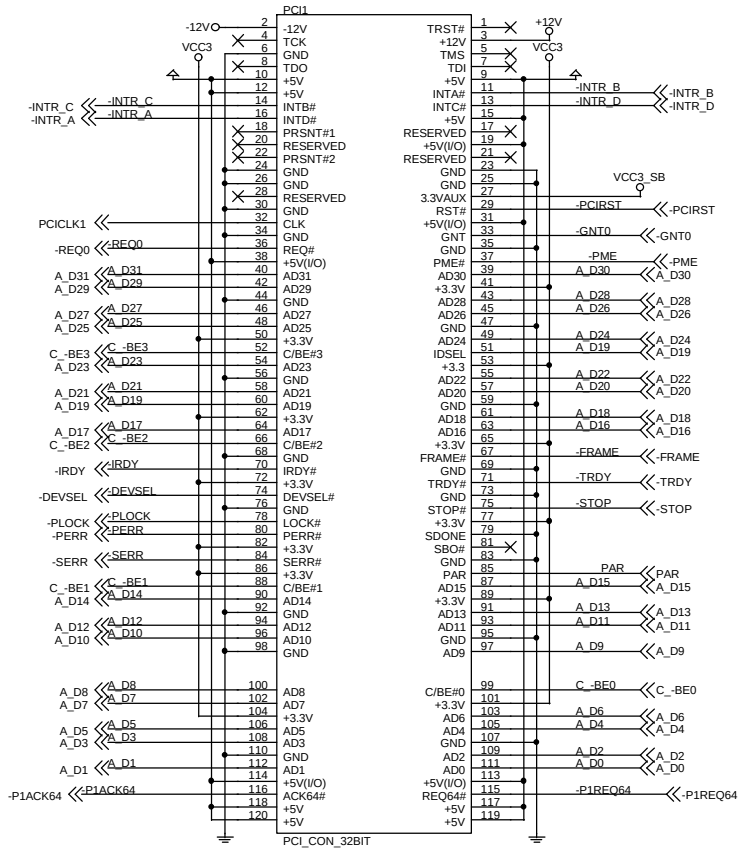


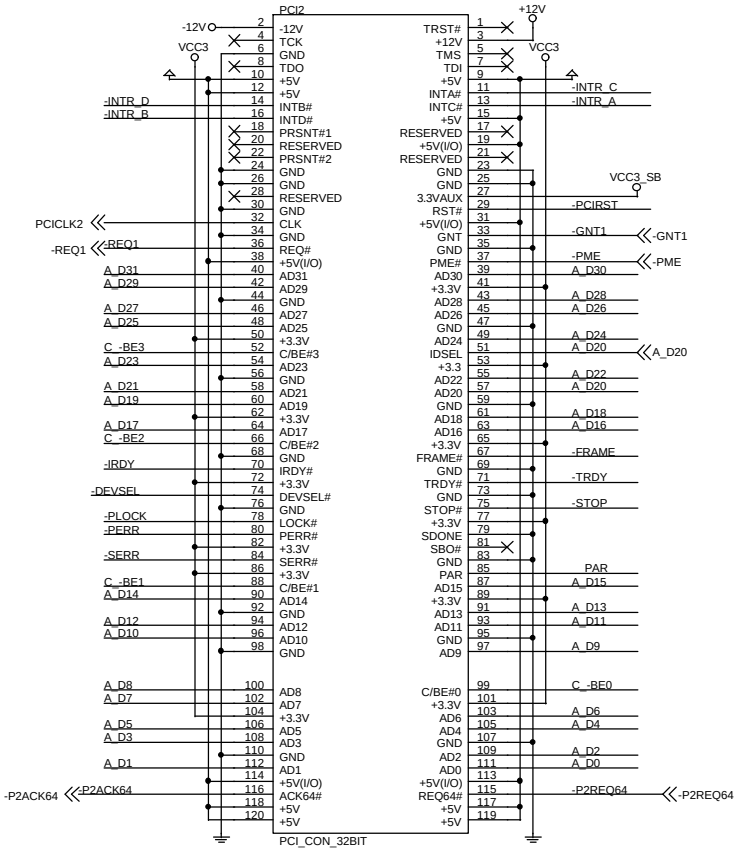
VIA TECHNOLOGIES, INC.

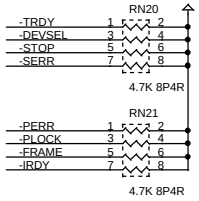
Title: SDRAM/LAN,MODEM WAKE UP FUNCTION

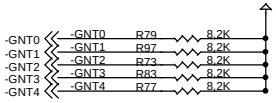
Size	Document Number	Rev
C	VT5228C (Preliminary)	0.1

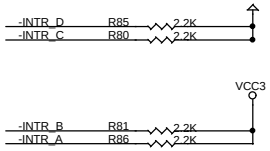
Date: Wednesday, November 24, 1999 Sheet 9 of 20

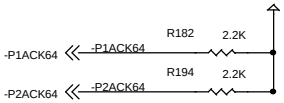


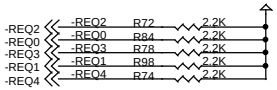










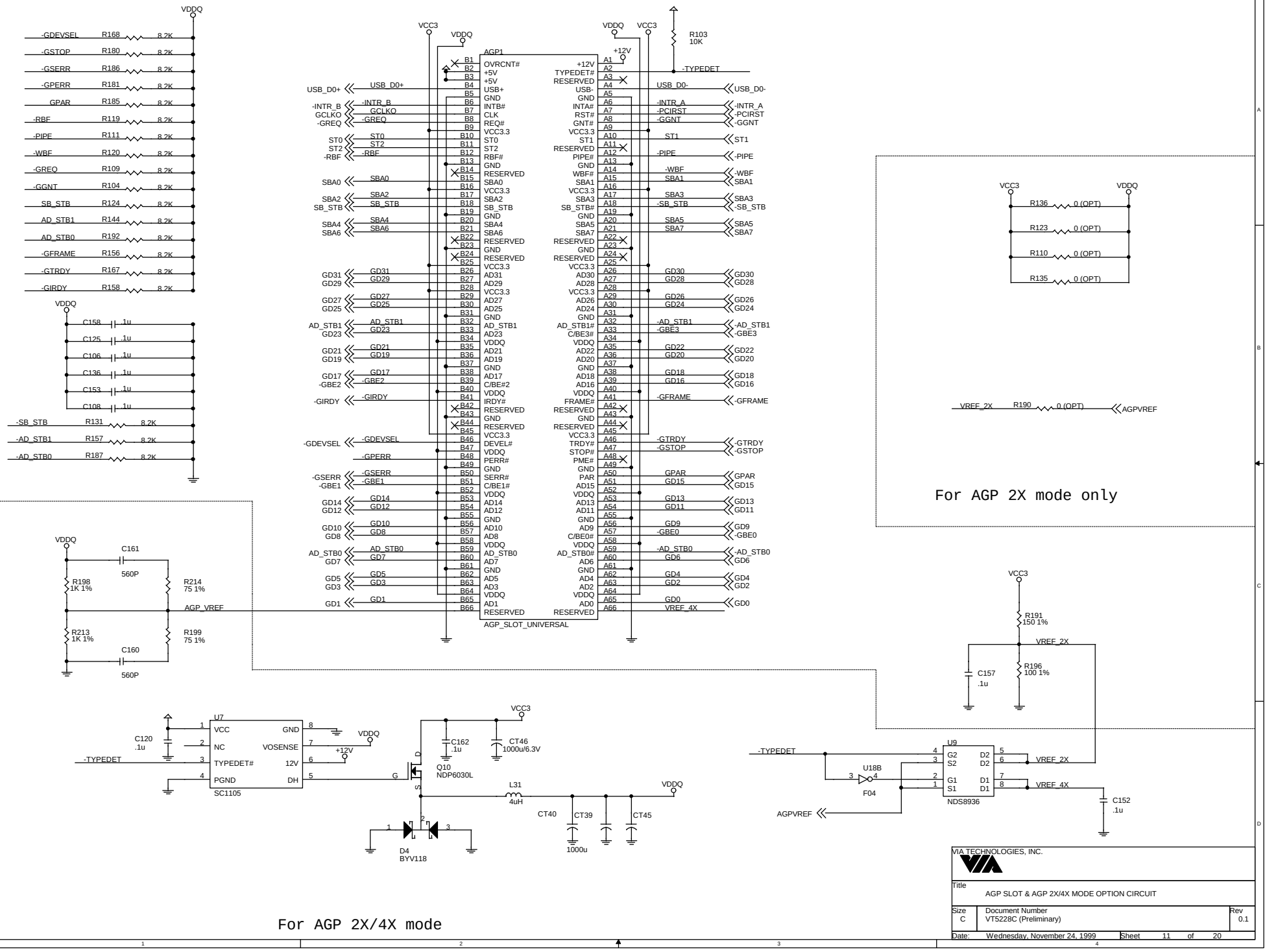


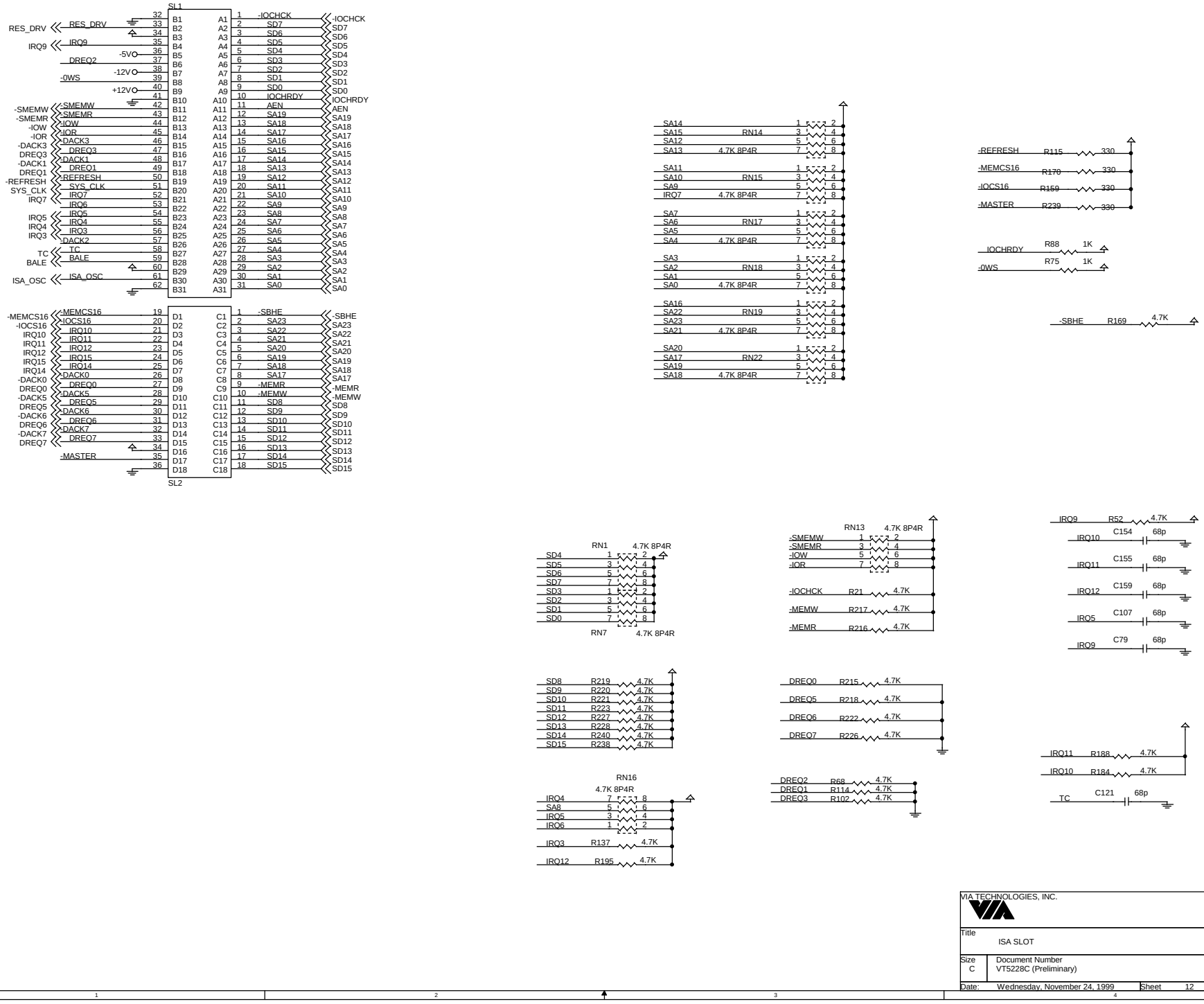
VIA TECHNOLOGIES, INC.

Title: PCI SLOT

Size	Document Number	Rev
C	VT5228C (Preliminary)	0.1

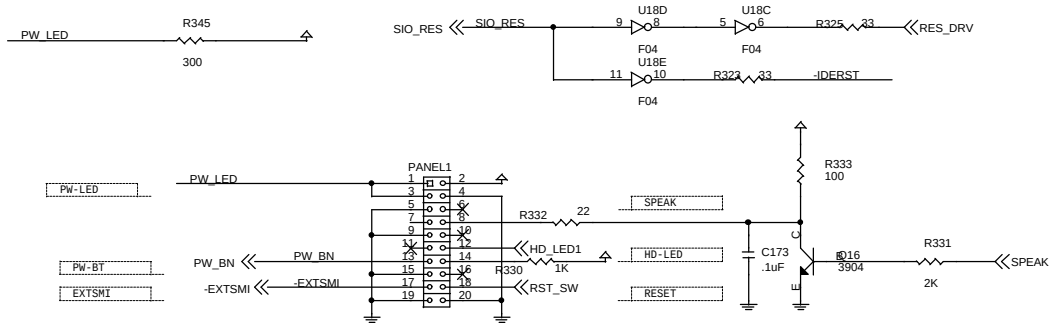
Date: Wednesday, November 24, 1999 Sheet 10 of 20

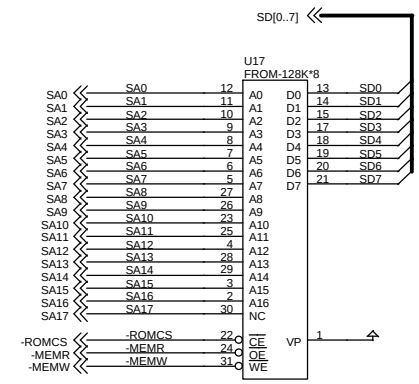

VDDQ
-GDEVSEL R168 8.2K
-GSTOP R180 8.2K
-GSERR R186 8.2K
-GPERR R181 8.2K
GPAR R185 8.2K
-RBF R119 8.2K
-PIPE R111 8.2K
-WBF R120 8.2K
-GREQ R109 8.2K
-GGNT R104 8.2K
SB_STB R124 8.2K
AD_STB1 R144 8.2K
AD_STB0 R192 8.2K
-GFRAME R156 8.2K
-GTRDY R167 8.2K
-GIRDY R158 8.2K
C158 1u
C125 1u
C106 1u
C136 1u
C153 1u
C108 1u
-SB_STB R131 8.2K
-AD_STB1 R157 8.2K
-AD_STB0 R187 8.2K
VCC3
AGP1
OVRCNT# +12V
+5V TYPEDET#
+5V RESERVED
USB+ USB-
GND GND
INTB# INTA#
CLK RST#
REQ# GNT#
VCC3.3 VCC3.3
ST0 ST1
ST2 RESERVED
RBF# PIPE#
GND GND
RESERVED WBF#
SBA0 SBA1
VCC3.3 VCC3.3
SBA2 SBA3
SB_STB SB_STB#
GND GND
SBA4 SBA5
SBA6 SBA7
RESERVED RESERVED
GND GND
RESERVED RESERVED
VCC3.3 VCC3.3
AD31 AD30
AD29 AD28
VCC3.3 VCC3.3
AD27 AD26
AD25 AD24
GND GND
AD_STB1 AD_STB1#
AD23 C/BE3#
VDDQ VDDQ
AD21 AD22
AD19 AD20
GND GND
AD17 AD18
C/BE#2 AD16
VDDQ VDDQ
IRDY# FRAME#
RESERVED RESERVED
GND GND
RESERVED RESERVED
VCC3.3 VCC3.3
DEVEL# TRDY#
VDDQ STOP#
PERR# PME#
GND GND
SERR# PAR
C/BE1# AD15
VDDQ VDDQ
AD14 AD13
AD12 AD11
GND GND
AD10 AD9
AD8 C/BE0#
VDDQ VDDQ
AD_STB0 AD_STB0#
AD7 AD6
GND GND
AD5 AD4
AD3 AD2
VDDQ VDDQ
AD1 AD0
RESERVED RESERVED
AGP_SLOT_UNIVERSAL
R103 10K
-TYPEDET
USB_D0+ USB_D0-
-INTR_B -INTR_A
GCLKO -PCIRST
-GREQ -GGNT
ST0 ST1
ST2 -PIPE
-RBF -WBF
SBA0 SBA1
SBA2 SBA3
SB_STB -SB_STB
SBA4 SBA5
SBA6 SBA7
GD31 GD30
GD29 GD28
GD27 GD26
GD25 GD24
AD_STB1 -AD_STB1
GD23 -GBE3
GD21 GD22
GD19 GD20
GD17 GD18
-GBE2 GD16
-GIRDY -GFRAME
-GDEVSEL -GTRDY
-GSTOP
-GPERR
-GSERR GPAR
-GBE1 GD15
GD14 GD13
GD12 GD11
GD10 GD9
GD8 -GBE0
AD_STB0 -AD_STB0
GD7 GD6
GD5 GD4
GD3 GD2
GD1 GD0
VREF_4X
For AGP 2X mode only
VCC3
VDDQ
R136 0 (OPT)
R123 0 (OPT)
R110 0 (OPT)
R135 0 (OPT)
VREF_2X R190 0 (OPT) AGPVREF
VDDQ
C161
560P
R198 1K 1%
R214 75 1%
AGP_VREF
R213 1K 1%
R199 75 1%
C160
560P
VCC3
R191 150 1%
VREF_2X
C157 .1u
R196 100 1%
U7
VCC GND
NC VOSENSE
TYPEDET# 12V
PGND DH
SC1105
C120 .1u
-TYPEDET
VDDQ
+12V
C162 .1u
CT46 1000u/6.3V
Q10 NDP6030L
G
D
S
L31 4uH
VDDQ
CT40 CT39 CT45
1000u
D4 BYV118
-TYPEDET
U18B
F04
U9
G2 D2
S2 D2
G1 D1
S1 D1
NDS8936
VREF_2X
VREF_4X
AGPVREF
C152 .1u
For AGP 2X/4X mode
VIA TECHNOLOGIES, INC.
Title
AGP SLOT & AGP 2X/4X MODE OPTION CIRCUIT
Size C
Document Number VT5228C (Preliminary)
Rev 0.1
Date: Wednesday, November 24, 1999
Sheet 11 of 20

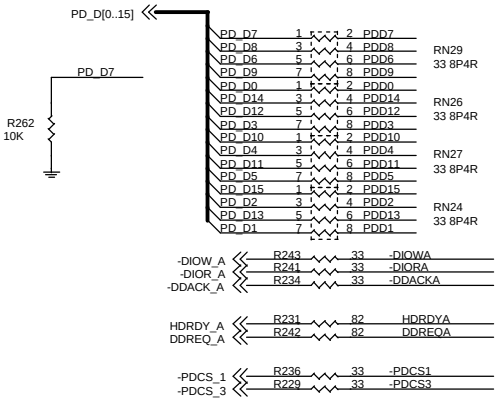


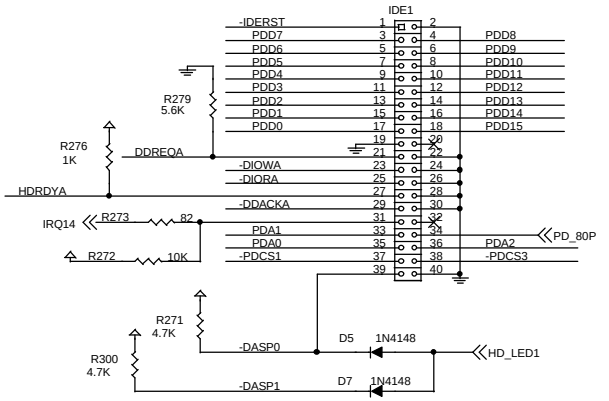
VIA TECHNOLOGIES, INC.

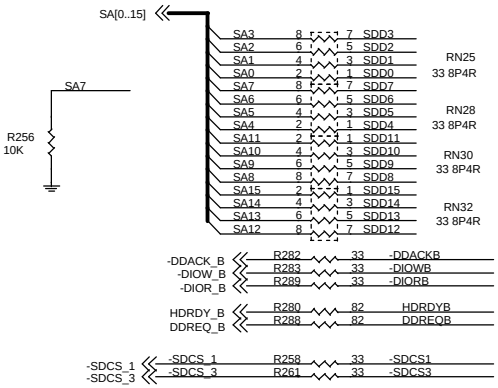
Title: ISA SLOT		
Size: C	Document Number: VT5228C (Preliminary)	Rev: 0.1
Date: Wednesday, November 24, 1999	Sheet 12 of 20	

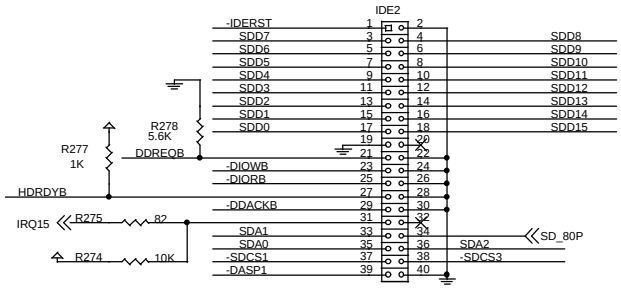


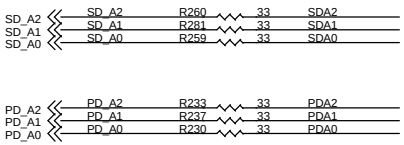




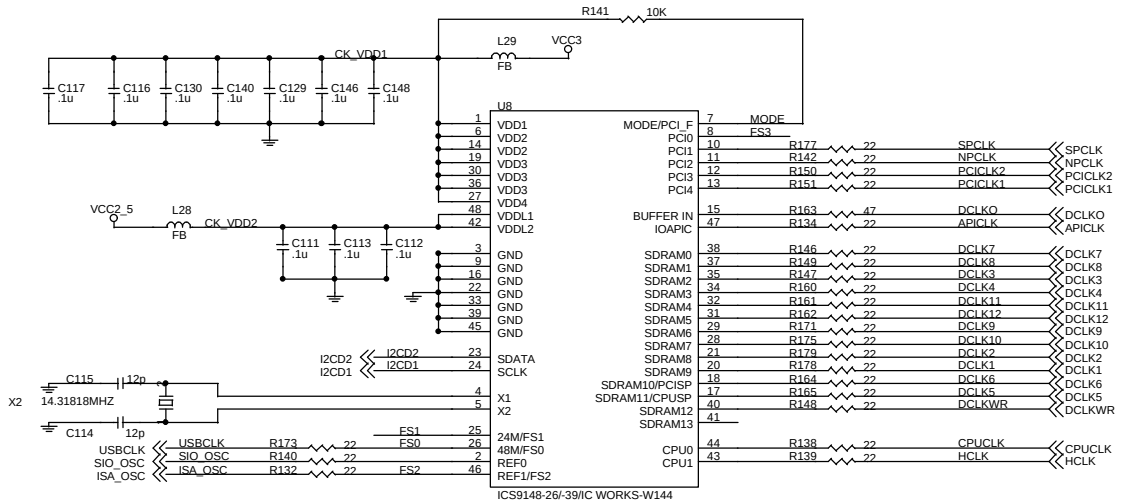


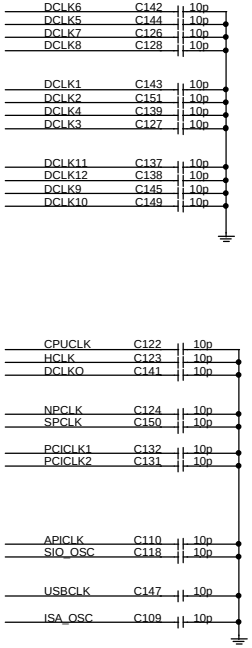


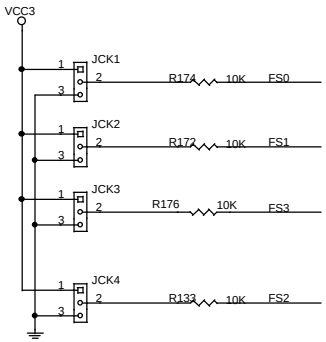


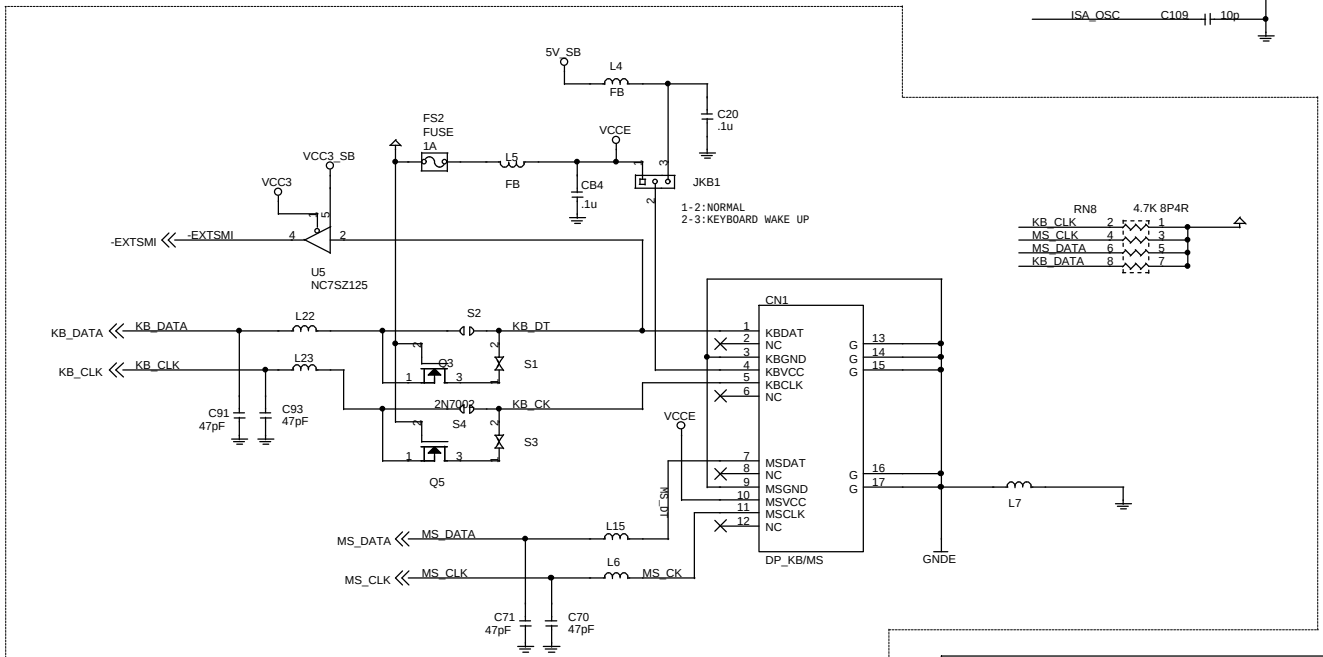


VIA TECHNOLOGIES, INC.		
Title: IDE/PANEL		
Size: C	Document Number: VT5228C (Preliminary)	Rev: 0.1
Date: Wednesday, November 24, 1999	Sheet 13 of 20	









JCK4	JCK3	JCK2	JCK1	CPU FREQ.	PCI
2-3	2-3	1-2	1-2	66.8MHz	33.3MHz
1-2	2-3	1-2	1-2	100.2MHz	33.3MHz
1-2	2-3	1-2	2-3	133MHz	44.4MHz
1-2	2-3	2-3	1-2	112MHz	37.3MHz
1-2	2-3	2-3	2-3	103MHz	34.3MHz
1-2	1-2	1-2	1-2	133MHz	33.3MHz
1-2	1-2	1-2	2-3	124MHz	31MHz
1-2	1-2	2-3	1-2	150MHz	37.5MHz
1-2	1-2	2-3	2-3	140MHz	35MHz

*For ICS 9148-39/IC WORKS-144

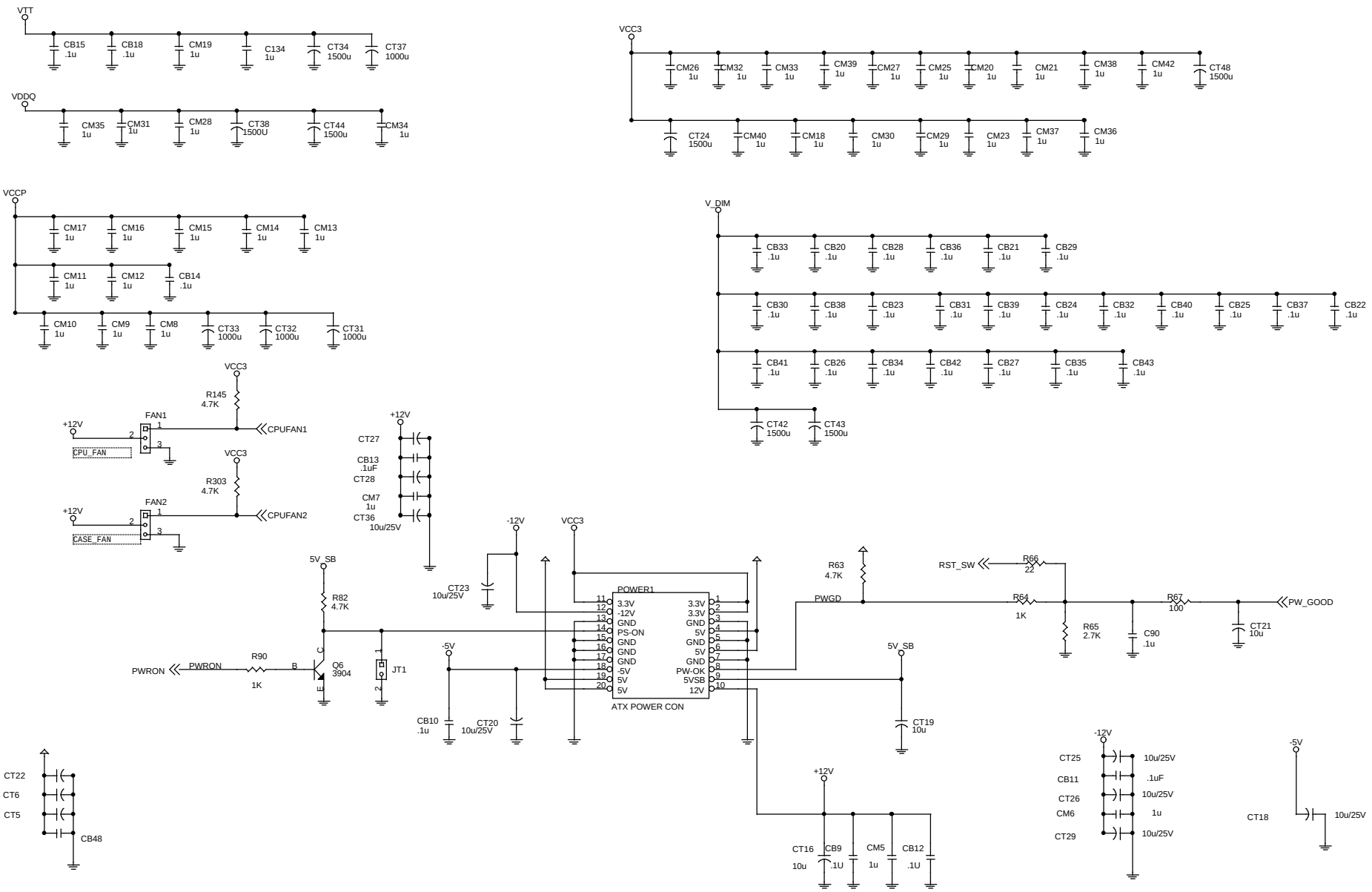
KEYBOARD WAKE UP

VIA TECHNOLOGIES, INC.

Title: CLOCK SYNTHESIZER/KB WAKE UP FUNCTION

Size	Document Number	Rev
C	VT5228C (Preliminary)	0.1

Date: Wednesday, November 24, 1999 Sheet 14 of 20

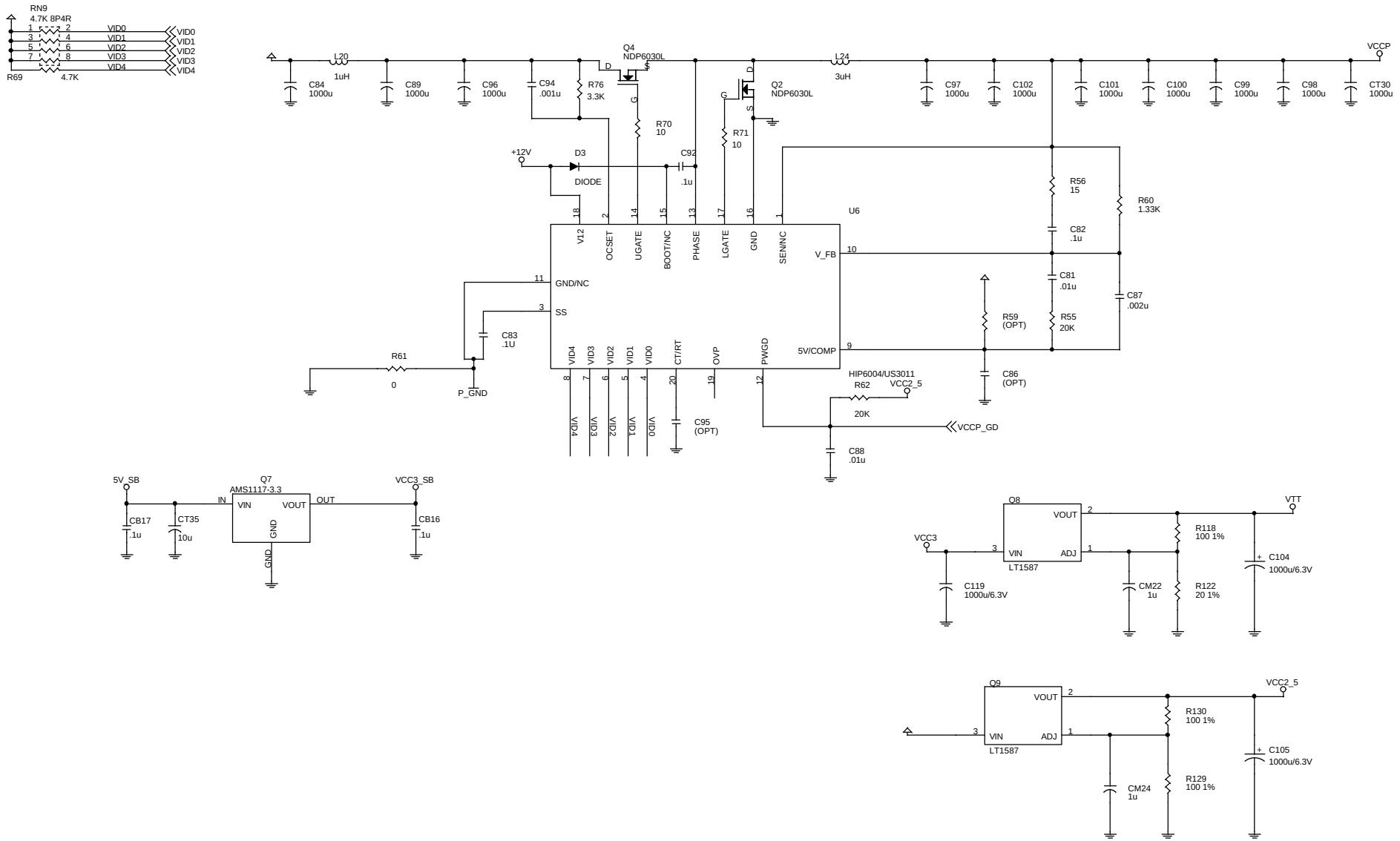


VIA TECHNOLOGIEA, INC.

Title: POWER CONNECTOR / BYPASS CAPACITORS

Size	Document Number	Rev
C	VT5228C (Preliminary)	0.1

Date: Wednesday, November 24, 1999 Sheet 15 of 20

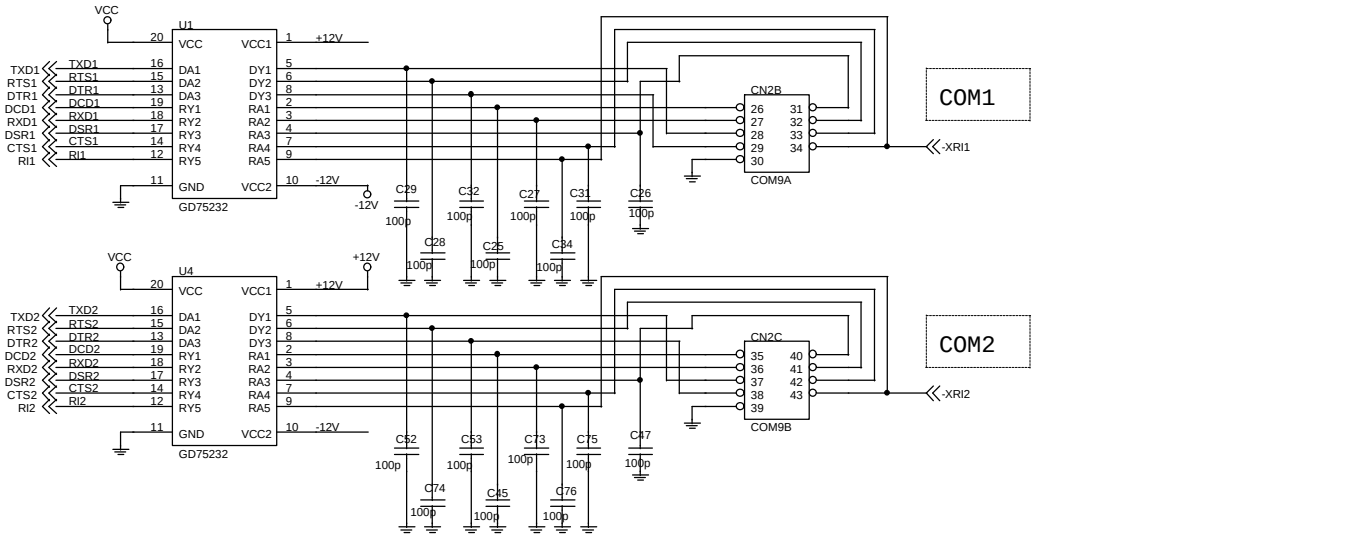


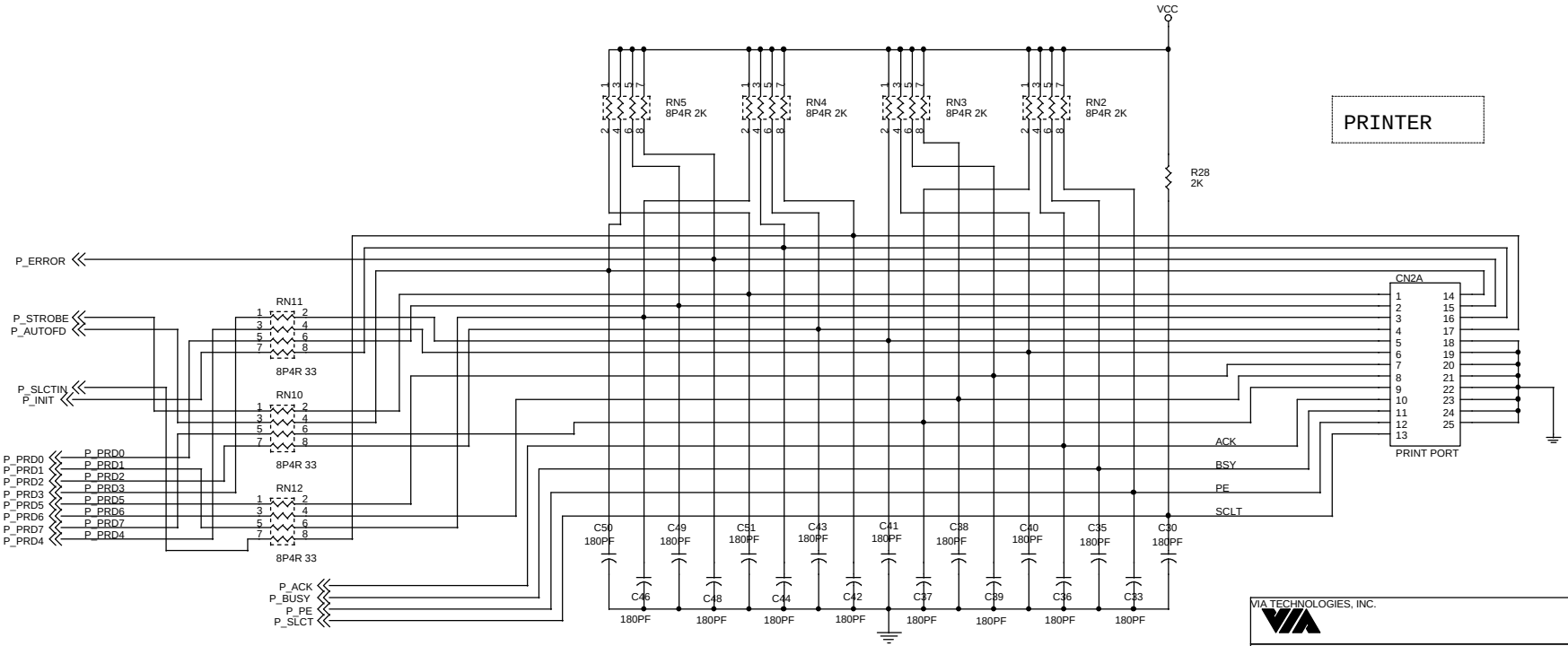
VIA TECHNOLOGIES, INC.

Title	DC-DC CONVERTER	
Size C	Document Number VT5228C (Preliminary)	Rev 0.1
Date: Wednesday, November 24, 1999	Sheet 16 of 20	

COM1, COM2 AND IR

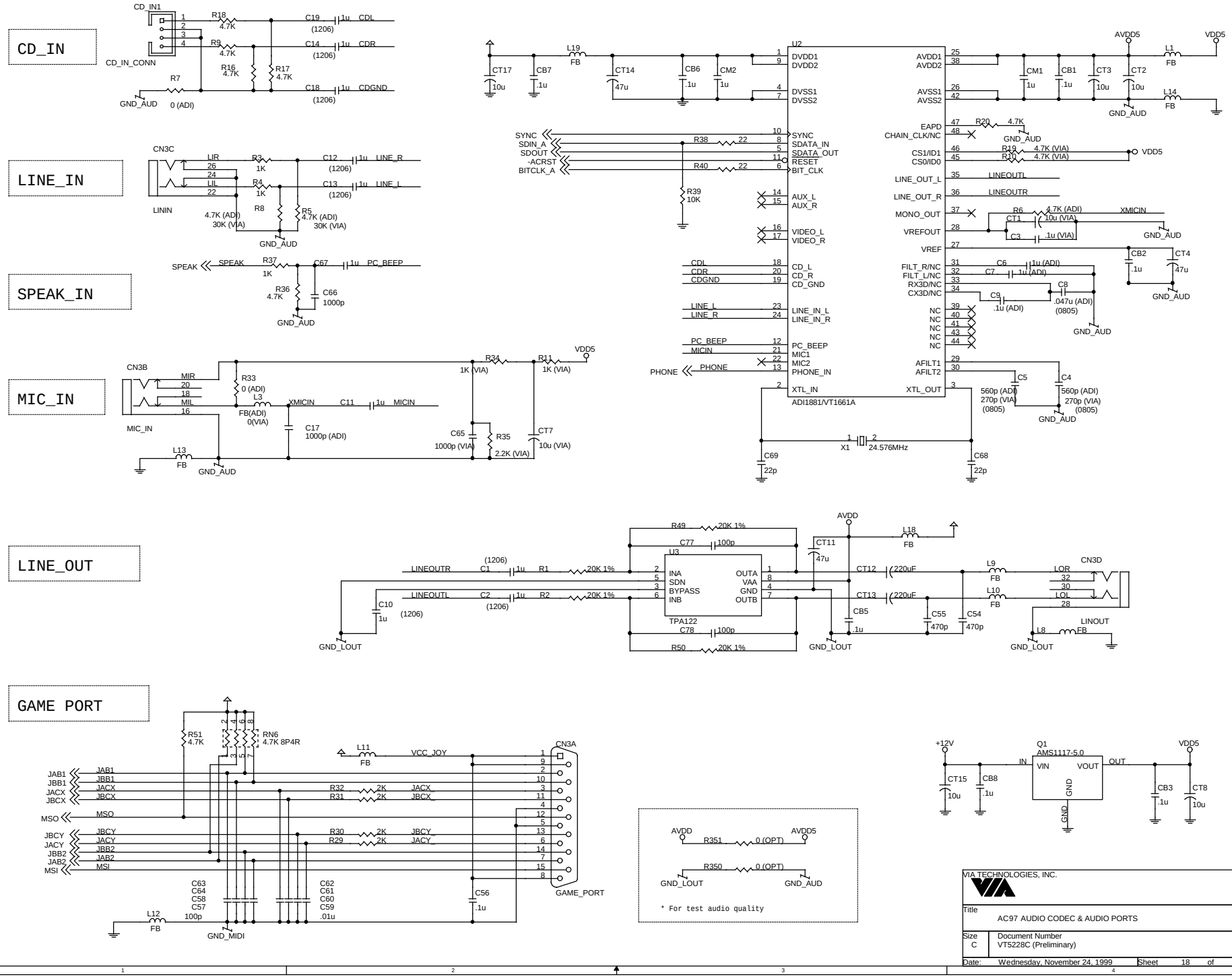
with Bipolar drivers and receivers

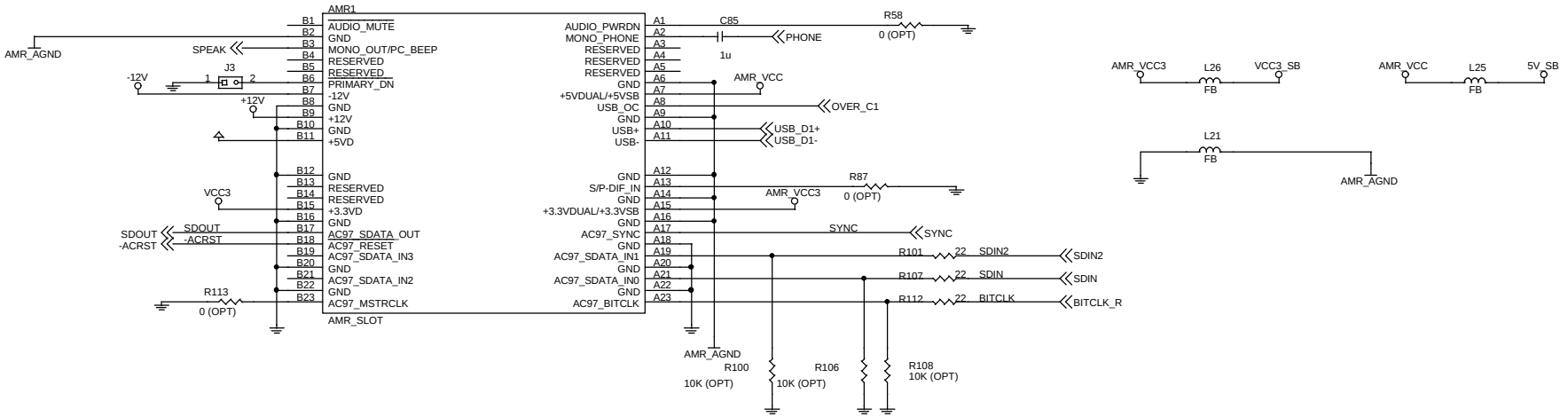




VIA TECHNOLOGIES, INC.

Title	PRINTER / COM PORT	
Size C	Document Number VT5228C (Preliminary)	Rev 0.1
Date: Wednesday, November 24, 1999	Sheet 17 of 20	


CD_IN
LINE_IN
SPEAK_IN
MIC_IN
LINE_OUT
GAME PORT
CD_IN1
CD_IN_CONN
GND_AUD
0 (ADI)
CN3C
LININ
4.7K (ADI)
30K (VIA)
SPEAK
PC_BEEP
CN3B
MIC_IN
FB(ADI)
0(VIA)
XMICIN
MICIN
1K (VIA)
2.2K (VIA)
U2
ADI1881/VT1661A
DVDD1
DVDD2
DVSS1
DVSS2
AVDD1
AVDD2
AVSS1
AVSS2
AVDD5
VDD5
SYNC
SDIN_A
SDOUT
-ACRST
BITCLK_A
SDATA_IN
SDATA_OUT
RESET
BIT_CLK
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_R
CD_GND
LINE_IN_L
LINE_IN_R
PC_BEEP
MIC1
MIC2
PHONE_IN
PHONE
XTL_IN
XTL_OUT
X1
24.576MHz
EAPD
CHAIN_CLK/NC
CS1/ID1
CS0/ID0
LINE_OUT_L
LINE_OUT_R
MONO_OUT
VREFOUT
VREF
FILT_R/NC
FILT_L/NC
RX3D/NC
CX3D/NC
AFILT1
AFILT2
LINEOUTL
LINEOUTR
U3
TPA122
INA
SDN
BYPASS
INB
OUTA
VAA
GND
OUTB
LINEOUTR
LINEOUTL
AVDD
CN3D
LOR
LOL
LINOUT
GND_LOUT
RN6
4.7K 8P4R
VCC_JOY
CN3A
GAME_PORT
JAB1
JBB1
JACX
JBCX
MSO
JBCY
JACY
JBB2
JAB2
MSI
GND_MIDI
+12V
Q1
AMS1117-5.0
IN
VIN
VOUT
OUT
GND
R351
R350
0 (OPT)
* For test audio quality
VIA TECHNOLOGIES, INC.
Title
AC97 AUDIO CODEC & AUDIO PORTS
Size
C
Document Number
VT5228C (Preliminary)
Rev
0.1
Date:
Wednesday, November 24, 1999
Sheet
18
of
20



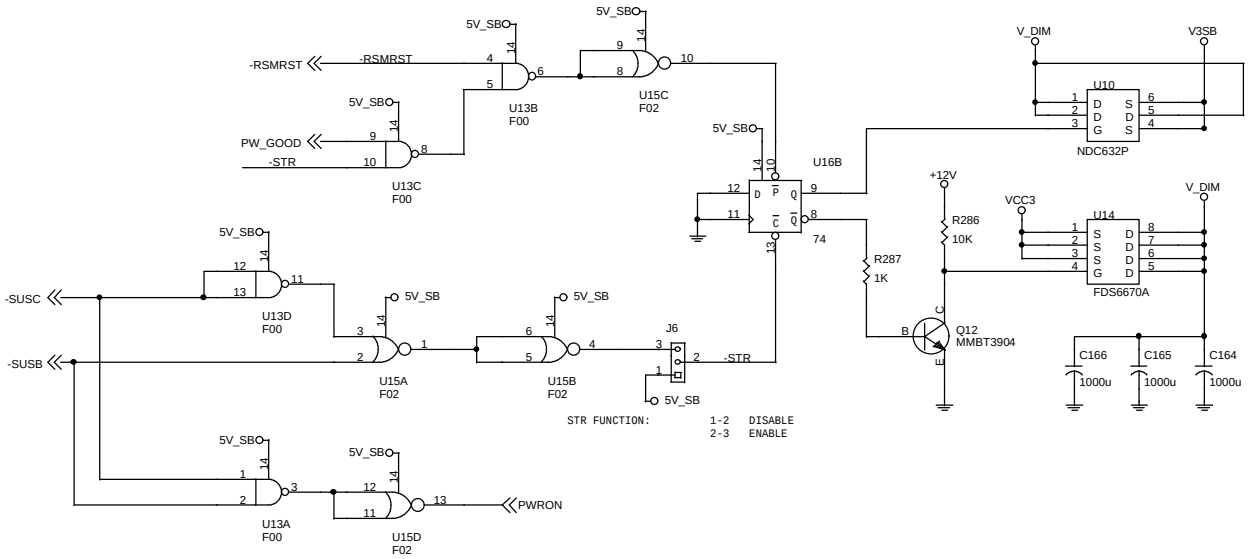
VIA TECHNOLOGIES, INC.

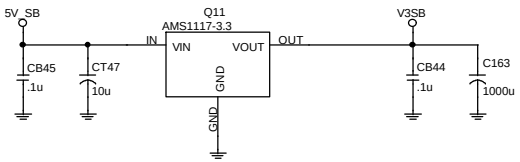
Title: AMR SLOT

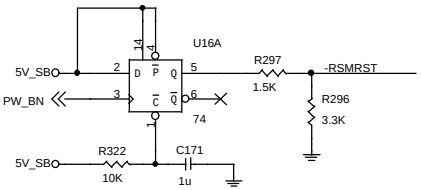
Size	Document Number	Rev
C	VT5228C (Preliminary)	0.1

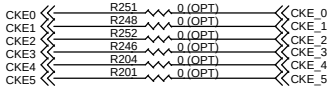
Date: Wednesday, November 24, 1999 Sheet 19 of 20

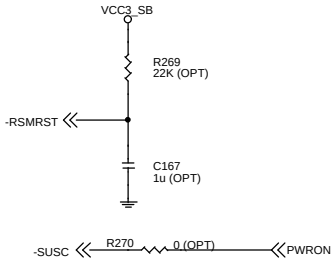
For STR function

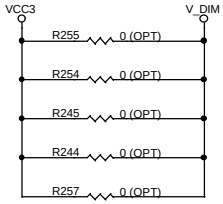


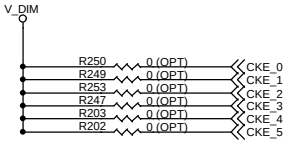












For NON-STR function

VIA TECHNOLOGIES, INC.		
Title: STR OPTION CIRCUIT		
Size: C	Document Number: VT5228C (Preliminary)	Rev: 0.1
Date: Wednesday, November 24, 1999	Sheet 20 of 20	